**DEPARTMENT OF COMPUTER SCIENCE ENGINEERING**



**LESSON PLAN**

**SUBJECT: COMPUTER SYSTEM ARCHITECHTURE**

**BRANCH: 3RD SEM, CSE**

**FACULTY NAME: DR. ANITARANI BRAHMA**

**Government Polytechnic Bargarh**

**OBJECTIVE:**

After completion of this course the student will be able to:

• Understand the basic structure of a computer with instructions.

• Learn about machine instructions and program execution.

• Learn about the internal functional units of a processor and how they are interconnected.

• Understand how I/O transfer is performed.

• Learn about basic memory circuit, organization and secondary storage.

• Understand concept of parallel processing.

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| **Branch: Computer Science Engineering** | **Name of the Faculty: Dr. Anitarani Brahma** | |  |  |
| **Sem: 3rd** | **No. of periods per week: 04 No. of week: 15 No. of periods: 60** | |  |  |
| **Subject: Computer System Architechture** |  |  |
| **WEEK** | **CLASS** | **TOPIC** | **SUBTOPICS COVERED** | **TEACHING MODES** |
| 1 | 1 | 1.1 Basic Structure of Computer hardware | Overview of Computer systems, historical evolution | PPT |
|  | 2 | Basic Structure and Componets | PPT |
|  | 3 | 1.2 Functional Units | Input Unit, Output Unit, Storage Unit | PPT |
|  | 4 | 1.3 Computer Components | CPU, Motherboard, Peripheral devices | PPT |
| 2 | 5 | 1.4 Performance Measures | Clock speed, MIPS, FLOPS | CHALK & BOARD |
|  | 6 | 1.5 Memory addressing & Operations | Memory Hierachy, Addressing Modes | PPT |
|  | 7 | Quiz test |  | PPT |
|  | 8 | 2.1 Fundamentals to Instructions | Instruction set architecture (ISA) | CHALK & BOARD |
| 3 | 9 | 2.2Operands | Types of operands, Operand Storage | CHALK & BOARD |
|  | 10 | 2.3 Opcodes | Different types of opcode | CHALK & BOARD |
|  | 11 | 2.4Instruction Formats | Instruction formats, Types of Instruction format | PPT |
|  | 12 | 2.5Addressing Modes | Immediate, direct, indirect, register, etc. | PPT |
| 4 | 13 | PPT |
|  | 14 | Quiz test |  |  |
|  | 15 | Performance test |  | PPT |
|  | 16 | 3.1Register Files | Types of registers, Roles in CPU | CHALK & BOARD |
| 5 | 17 | CHALK & BOARD |
|  | 18 | 3.2 Instruction Execution Cycle | Fetch, decode, execute | CHALK & BOARD |
|  | 19 | Examples and practical scenarios | CHALK & BOARD |
|  | 20 | 3.3 Hardware Control | Control unit | CHALK & BOARD |
| 6 | 21 | Hardware Control | CHALK & BOARD |
|  | 22 | 3.4 Microprogram Control | Microinstructions, | CHALK & BOARD |
|  | 23 | Control Memory | CHALK & BOARD |
|  | 24 | Quiz test |  |  |
| 7 | 25 | 4.1 Memory Characteristics | Volatile vs Non-volatile | CHALK & BOARD |
|  | 26 | Characteristics | CHALK & BOARD |
|  | 27 | 4.2 Memory Hierarchy | Levels of memory | PPT |
|  | 28 | Speed and size trade-offs | PPT |
| 8 | 29 | 4.3 RAM and ROM Organization | Types and uses | CHALK & BOARD |
|  | 30 | 4.4 Interleaved Memory | Concept and advantages | CHALK & BOARD |
|  | 31 | 4.5 Cache Memory | Types | CHALK & BOARD |
|  | 32 | Mapping techniques | CHALK & BOARD |
| 9 | 33 | 4.6 Virtual Memory | Paging | CHALK & BOARD |
|  | 34 | Segmentation | CHALK & BOARD |
|  | 35 | Quiz test |  |  |
|  | 36 | 5.1 Input - Output Interface | I/O architecture | CHALK & BOARD |
| 10 | 37 | Ports and interfaces | CHALK & BOARD |
|  | 38 | 5.2 Modes of Data Transfer | Synchronous, asynchronous | CHALK & BOARD |
|  | 39 | Block transfer | CHALK & BOARD |
|  | 40 | 5.3 Programmed I/O Transfer | Polling | CHALK & BOARD |
| 11 | 41 | Characteristics | CHALK & BOARD |
|  | 42 | 5.4 Interrupt Driven I/O | Interrupts and handling | CHALK & BOARD |
|  | 43 | 5.5 I/O and Bus Systems | I/O and | CHALK & BOARD |
|  | 44 | Bus Systems | CHALK & BOARD |
| 12 | 45 | 5.6 DMA | Direct Memory Access,Applications | CHALK & BOARD |
|  | 46 | 5.7 I/O Processor | Functions and benefits | CHALK & BOARD |
|  | 47 | Quiz test |  |  |
|  | 48 | 6.1 Bus and System Bus | Basic concepts | PPT |
| 13 | 49 | 6.2 Types of System Bus | Data, address, control buses | PPT |
|  | 50 |  | PPT |
|  | 51 | 6.3 Bus Structure and Parameters | Bus design | PPT |
|  | 52 | SCSI and USB | PPT |
| 14 | 53 | 6.4 Advanced Bus Systems and Parallel Processing |  | CHALK & BOARD |
|  | 54 | Quiz test |  |  |
|  | 55 | 7.1 Parallel Processing | Concepts and architectures | CHALK & BOARD |
|  | 56 | 7.2 Linear Pipeline | Pipeline stages | CHALK & BOARD |
| 15 | 57 | 7.3 Multiprocessor Systems | SMP, MPP | CHALK & BOARD |
|  | 58 | 7.4 Flynn's Classification | SISD, SIMD | CHALK & BOARD |
|  | 59 | MISD, MIMD | CHALK & BOARD |
|  | 60 | Previous year questions |  |  |
|  |  |  |  |  |
| **Book Recommended:-** |  |  |  |  |
| 1 Moris Mano, Computer System Architecture, PHI | | |  |  |
| 2 Er. Rajeev Chopra, Computer Architecture and Organisation, S.Chand | | |  |  |
| 3 Parthasarthy, Senthil Kumar, Fundamentals of Computer Architecture, TMH | | |  |  |

Faculty Senior Lecturer