## GOVERNMENT POLYTECHNIC, BARGARH Department of ELECTRICAL AND ELECTRONICS Engineering

Semester: 3<sup>RD</sup>. DIPLOMA

Subject: Digital Electronics

No of Period: 45 (3p/week)

Branch: EEE

Name of Faculty: NIRANJAN NAYAK

Week	Period	Topics to be covered		
1 <sup>st</sup> Week	1	Introduction to Logic Gates Basic logic gates: OR, AND, and NOT and its		
		Truth tables.		
	2	Logic symbols, Logic voltage levels and Logic circuit design examples.		
	3	Integrated Circuits.		
2 <sup>nd</sup> Week	4	Design of NOR, NAND, Exclusive OR, and Exclusive NOR gates.		
	5	NOR and NAND gates used as inverters.		
	6	Fan-in and fan-out and Termination of unused inputs.		
3 <sup>rd</sup> Week	7	AND and OR gates constructed from NAND and NOR gates.		
	8	Boolean operations (OR, AND, NOT) and Representation of logic circuits by Boolean expressions.		
	9	Laws of Boolean algebra.		
		1. Double inversion: A"=A.		
		2. OR identities: $A+0 = A$ , $A+1=1$ , $A+A=A$ , $A+A'=1$ .		
		3. AND identities: A.0=0, A.1=A, A.A=A, A.A'=0.		
4th Maral	10	4.Cumulative laws: A+B=B+A, A.B=B.A.		
4 <sup>th</sup> Week	10	<ul> <li>5. Associative laws: (A+B) +C=A+ (B+C), (A.B).C=A.(B.C).</li> <li>6. Distributive laws: A+ (B.C) = (A+B).(A+C), A.(B+C)=A.B+A.C.</li> </ul>		
		7. DE Morgan's theorems.		
		(A+B+C+)'=A'.B'.C', (A.B.C)'=A'+B'+C'		
	11	Applications to logic circuit simplifications and design.		
	12	Equivalent logic gates and NAND and NOR implementations of logic circuits.		
5 <sup>th</sup> Week	13	Standard forms of Boolean expressions that is Sum-of-products (SOP) and		
_		Product-of-sums (POS).		
	14	Karnaugh mapping.		
	15	Construction and working of Half adder and Full adder.		
6 <sup>th</sup> Week	16	Construction and working of Half Subtractor and Full Subtractor.		
	17	Construction and working of 4 bit adder.		
	18	Construction and working of Multiplexer (4:1) and De-multiplexer (1:4).		
7 <sup>th</sup> Week	19	Construction and working of Decoder and Encoder.		
	20	Construction and working of Digital comparator (3 Bit) and Seven segment		
<u> </u>		Decoder.		
	21	Latches & Flip-Flops that is Basic latches NOR latch, NAND latch and		
		Example uses of latches.		

2. Gated D-latch.  1. Introduction to Flip-flops: 1. Master-slave and edge-triggered principles. 2. S-R flip-flop. 2. D-type flip-flop, J-K flip-flop. 24 D-type flip-flop, J-K flip-flop. 25 T-type flip-flop and Flip-flop timing diagrams. 26 Introduction to Counters. 1. Circuit diagram and working principle of Binary counters. 27 2. up-down counter (circuits, truth tables, and timing diagrams). 3. Asynchronous counters and ripple counter. 4. Synchronous counters and ripple counter. 5. Decade counter. 6. Module—1 counter and its combinations. 29 7. Divide-by-n counters obtained from truncated binary sequences. 8. Synchronous counter design using D-type flip-flops. 9. Synchronous counter design using J-K flip-flops. 10 Introduction to Shift Registers. 1. Circuit diagram, truth tables, and timing diagrams of Shift Registers. 1. Circuit diagram, truth tables, and timing diagrams of Shift Registers. 32 Serial/parallel load shift register. 33 Shift register counters. 1. Ring counter. 34 Serial input shift register. 35 Introduction to Semiconductor Memories. 1. Define the terms ROM, RAM, PROM, and EPROM. 2. Draw a typical memory cell. 2. Draw a typical memory cell. 38 Design as mall diode matrix ROM to serve as a code converter. 39 Operating principle of dynamic memory. 40 Advantages and disadvantages of dynamic memory vs. static memory. 41 Difference between dynamic memory vs. static memory. 42 Introduction to Sequential Circuit Design. 1. Combinational vs. Sequential Circuits. 44 Previous year question discussion. 45 Previous year question discussion.	8 <sup>th</sup> Week	22	Gated latches.  1. Gated S-R latch.
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