GOVT. POLYTECHNIC
BARGARH

LECTURE NOTE

POWER ELECTRONICS & PLC

SEMESTER-5TH

EE/EEE ENGINEERING

PREPARED BY

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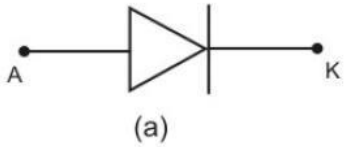
Chapter-1: Power Semiconductor devices

1.1 Power Diode

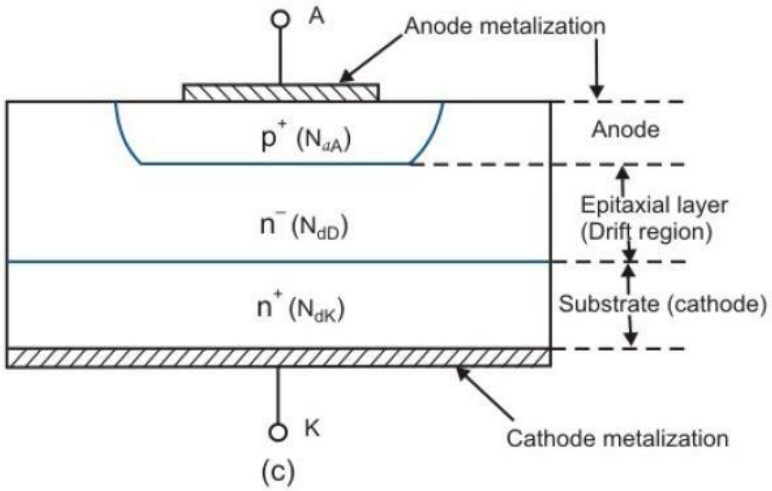
1.1.1 Explain the operation, construction & application of Power Diode

Power Diodes of largest power rating are required to conduct several kilo amps of current in the forward direction with very little power loss while blocking several kilo volts in the reverse direction. Large blocking voltage requires wide depletion layer in order to restrict the maximum electric field strength below the ‑impact ionization‖ level. Space charge density in the depletion layer should also be low in order to yield a wide depletion layer for a given maximum Electric fields strength. These two requirements will be satisfied in a lightly doped p-n junction diode of sufficient width to accommodate the required depletion layer. Such a construction, however, will result in a device with high resistively in the forward direction. Consequently, the power loss at the required rated current will be unacceptably high. On the other hand if forward resistance (and hence power loss) is reduced by increasing the doping level, reverse break down voltage will reduce. This apparent contradiction in the requirements of a power diode is resolved by introducing a lightly doped ‑drift layer‖ of required thickness between two heavily doped p and n layers as shown in Fig 1 (c). Fig 1 (a) and (b) shows the circuit symbol and the photograph of a typical power diode respectively.



(a)

(b)



(c)

Fig.1: Diagram of a power; (a) circuit symbol (b) photograph; (c) schematic cross

To arrive at the structure shown in Fig 1 (c) a lightly doped **n** epitaxial layer of specified width (depending on the required break down voltage) and donor atom density (N) is grown on a heavily doped **n+** substrate (NdK donor atoms. Cm-3) which acts as the cathode. Finally the **p-n** junction is formed by defusing a heavily doped (NaA acceptor atoms.Cm-3) **p+** region into the epitaxial layer. This **p** type region acts as the anode.

The different applications of Power Diode are in SMPs, Snubber, Chopper and freewheeling diode etc.

1.1.2 Explain V-I characteristics curve of Power Diode

Power Diodes take finite time to make transition from reverse bias to forward bias condition (switch ON) and vice versa (switch OFF). Behavior of the diode current and voltage during these switching periods are important due to the following reasons.

i) Severe over voltage / over current may be caused by a diode switching at different points in the circuit using the diode.

ii) Voltage and current exist simultaneously during switching operation of a diode. Therefore, every switching of the diode is associated with some energy loss. At high switching frequency this may contribute significantly to the overall power loss in the diode.

Observed Turn ON behavior of a power Diode: Diodes are often used in circuits with di/dt limiting inductors. The rate of rise of the forward current through the diode during Turn ON has significant effect on the forward voltage drop characteristics. A typical turn on transient is shown in Fig. 2

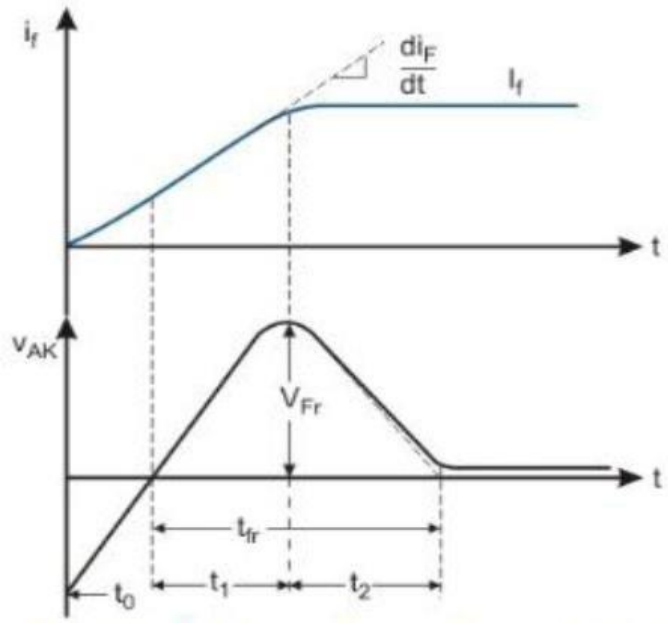


Fig. 2 : Forward current and voltage waveforms of a power diode during Turn On operation.

It is observed that the forward diode voltage during turn ON may transiently reach a significantly higher value Vfr compared to the steady slate voltage drop at the steady current IF . Vfr (called forward recovery voltage) is given as a function of the forward di/dt in the manufacturer‘s data sheet. Typical values lie within the range of 10-30V. Forward recovery time (tfr) is typically within 10 us.

Observed Turn OFF behavior of a Power Diode: Figure 3 shows a typical turn off behavior of a power diode assuming controlled rate of decrease of the forward current.

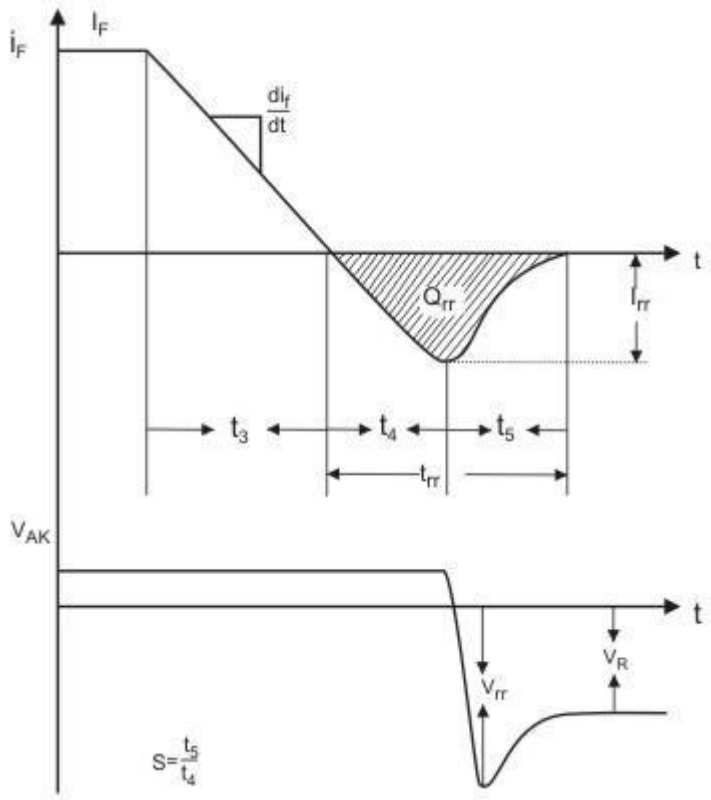


Fig. 3: Reverse Recovery characteristics of a power diode

Salient features of this characteristic are:

The diode current does not stop at zero, instead it grows in the negative direction to Irr called ‑peak reverse recovery current‖ which can be comparable to IF. In many power electronic circuits (e.g. choppers, inverters) this reverse current flows through the main power switch in addition to the load current. Therefore, this reverse recovery current has to be accounted for while selecting the main switch.

Voltage drop across the diode does not change appreciably from its steady state value till the diode current reaches reverse recovery level. In many power electric circuits (choppers, inverters) this may create an effective short circuit across the supply, current being limited only by the stray wiring inductance. Also in high frequency switching circuits (e.g, SMPS) if the time period t4 is comparable to switching cycle qualitative modification to the circuit behavior is possible.

Towards the end of the reverse recovery period if the reverse current falls too sharply, (low value of S), stray circuit inductance may cause dangerous over voltage (Vrr) across the device. It may be required to protect the diode using an RC snubber.

During the period t5 large current and voltage exist simultaneously in the device. At high switching frequency this may result in considerable increase in the total power loss.

1.2 SCR

1.2.1 Layer diagram of SCR and operation & construction of SCR.

Thyristors (also known as the Silicon Controlled Rectifiers or SCRs)

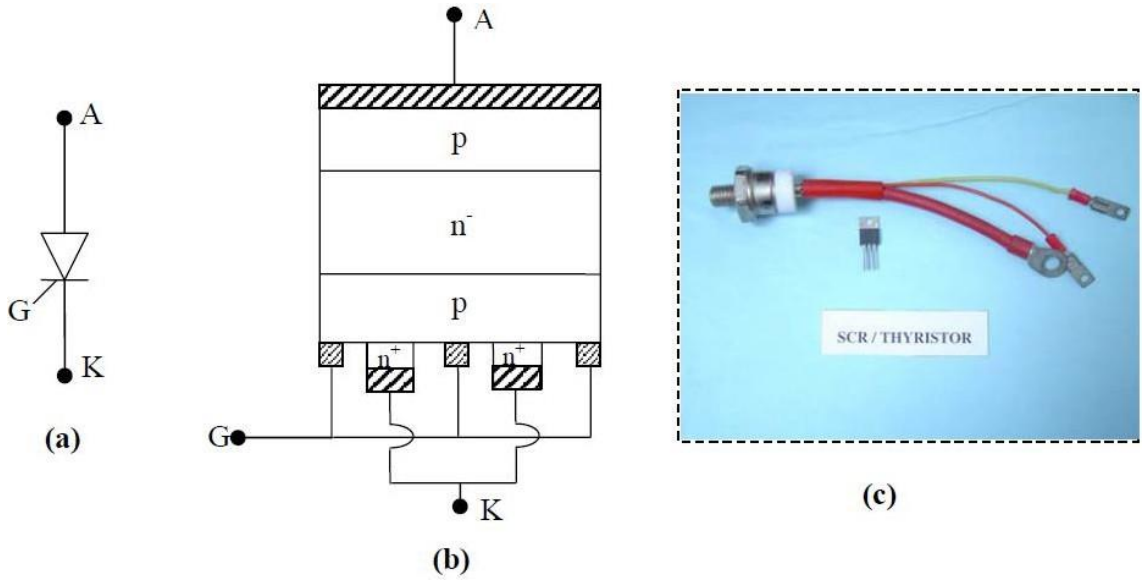


Fig. 4.1: Constructional features of a thysistor
(a) Circuit Symbol, (b) Schematic Construction, (c) Photograph

As shown in Fig 4.1 (b) the primary crystal is of lightly doped $\mathbf{n^-}$ type on either side of which two **p** type layers with doping levels higher by two orders of magnitude are grown. As in the case of power diodes and transistors, depletion layer spreads mainly into the lightly doped $\mathbf{n^-}$ region. The thickness of this layer is therefore determined by the required blocking voltage of the device. However, due to conductivity modulation by carriers from the heavily doped p regions on both side during ON condition the ‑ON state‖ voltage drop is less. The outer n^+ layers are formed with doping levels higher then both the p type layers. The top **p** layer acls as the ‑Anode‖ terminal while the bottom $\mathbf{n^+}$ layers acts as the ‑Cathode‖. The ‑Gate‖ terminal connections are made to the bottom **p** layer.

For better switching performance it is required to maximize the peripheral contact area of the gate and the cathode regions. Therefore, the cathode regions are finely distributed between gate contacts of the **p** type layer. An ‑Involute‖ structure for both the gate and the cathode regions is a preferred design structure.

1.2.2 Explain the two transistor analogy of SCR

Basic operating principle of a thyristor

The underlying operating principle of a thyristor is best understood in terms of the ‑two transistor analogy‖ as explained below.

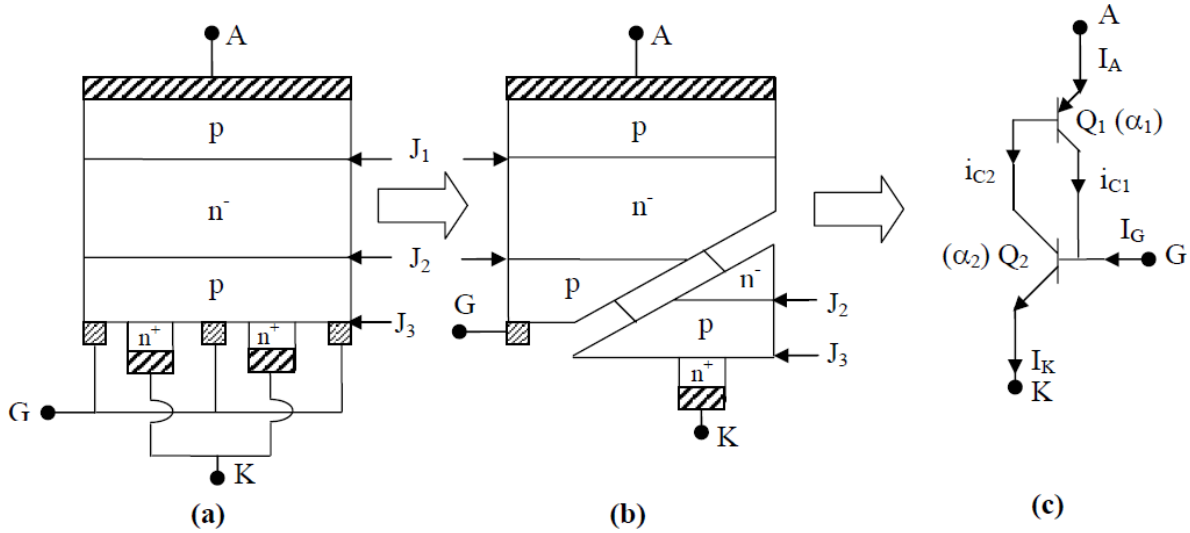


Fig. 4.2: Two transistor analogy of a thyristor construction.
(a) Schematic Construction, (b) Schematic division in component transistor
(c) Equivalent circuit in terms of two transistors.

a) Schematic construction,

b) Schematic division in component transistor

c) Equivalent circuit in terms of two transistors.

Let us consider the behavior of this p n p n device with forward voltage applied, i.e anode positive with respect to the cathode and the gate terminal open. With this voltage polarity J_1 & J_3 are forward biased while J_2 reverse biased.

Under this condition.

$$ic_1 = \alpha_1 I_A + I_{co1} \qquad (4.1)$$

$$ic_2 = \alpha_2 I_K + I_{co2} \qquad (4.2)$$

Where a_1 & a_2 are current gains of Q_1 & Q_2 respectively while I_{co1} & I_{co2} are reverse saturation currents of the CB junctions of Q_1 & Q_2 respectively.

Now from Fig 4.2 (c).

$$i_{c1} + i_{c2} = I_A \quad (4.3)$$

$$\& \; I_A = I_K \quad (4.4) \; (\because I_G = 0)$$

Combining Eq 4.1 & 4.4

$$I_A = \frac{I_{co1} + I_{co2}}{1 - (\alpha_1 + \alpha_2)} = \frac{I_{co}}{1 - (\alpha_1 + \alpha_2)} \quad (4.5)$$

Where $I_{co} \triangleq I_{co1} + I_{co2}$ is the total reverse leakage current of J_2

Now as long as V_{AK} is small I_{co} is very low and both a_1 & a_2 are much lower than unity. Therefore, total anode current I_A is only slightly greater than I_{co}. However, as V_{AK} is increased up to the avalanche break down voltage of J_2, I_{co} starts increasing rapidly due to avalanche multiplication process. As I_{co} increases both a_1 & a_2 increase and $a_1 + a_2$ approaches unity. Under this condition large anode current starts flowing, restricted only by the external load resistance. However, voltage drop in the external resistance causes a collapse of voltage across the thyristor. The CB junctions of both Q_1 & Q_2 become forward biased and the total voltage drop across the device settles down to approximately equivalent to a diode drop. The thyristor is said to be in ―ON‖ state.

Just after turn ON if I_a is larger than a specified current called the Latching Current I_L, a_1 and a_2 remain high enough to keep the thyristor in ON state. The only way the thyristor can be turned OFF is by bringing I_A below a specified current called the holding current (I_H) where upon a_1 & a_2 starts reducing. The thyristor can regain forward blocking capacity once excess stored charge at J_2 is removed by application of a reverse voltage across A & K (ie, K positive with respect A).

It is possible to turn ON a thyristor by application of a positive gate current (flowing from gate to cathode) without increasing the forward voltage across the device up to the forward break-over level. With a positive gate current equation 4.4 can be written as

$$I_K = I_A + I_G \quad (4.6)$$

Combining with Eqns. 4.1 to 4.3 $\quad I_A = \frac{\alpha_2 I_G + I_{co}}{1 - (\alpha_1 + \alpha_2)} \quad (4.7)$

Obviously with sufficiently large I_G the thyristor can be turned on for any value of I_{co} (and hence V_{AK}). This is called gate assisted turn on of a Thyristor. This is the usual method by which a thyristor is turned ON.

When a reverse voltage is applied across a thyristor (i.e, cathode positive with respect to anose.) junctions J_1 and J_3 are reverse biased while J_2 is forward biased. Of these, the junction J_3 has a very low reverse break down voltage since both the $\mathbf{n^+}$ and **p** regions on either side of this junction are heavily doped. Therefore, the applied reverse voltage is almost entirely supported by junction J_1. The maximum value of the reverse voltage is restricted by

a) The maximum field strength at junction J_1 (avalanche break down)

b) Punch through of the lightly doped n^- layer.

Since the **p** layers on either side of the $\mathbf{n^-}$ region have almost equal doping levels the avalanche break down voltage of J_1 & J_2 are almost same. Therefore, the forward and the reverse break down voltage of a thyristor are almost equal.Up to the break down voltage of J_1 the reverse current of the thyristor remains practically constant and increases sharply after this voltage. Thus, the reverse characteristics of a thyristor is similar to that of a single diode.

If a positive gate current is applied during reverse bias condition, the junction J_3 becomes forward biased. In fact, the transistors Q_1 & Q_2 now work in the reverse direction with the roles of their respective emitters and collectors interchanged. However, the reverse a_1 & a_2 being significantly smaller than their forward counterparts latching of the thyristor does not occur. However, reverse leakage current of the thyristor increases considerably increasing the OFF state power loss of the device.

If a forward voltage is suddenly applied across a reverse biased thyristor, there will be considerable redistribution of charges across all three junctions. The resulting current can become large enough to satisfy the condition $a_1 + a_2 = 1$ and consequently turn on the thyristor. This is called dvdt turn on of a thyristor and should be avoided.

1.2.3 Static V-I characteristics & Dynamic characteristics of SCR.

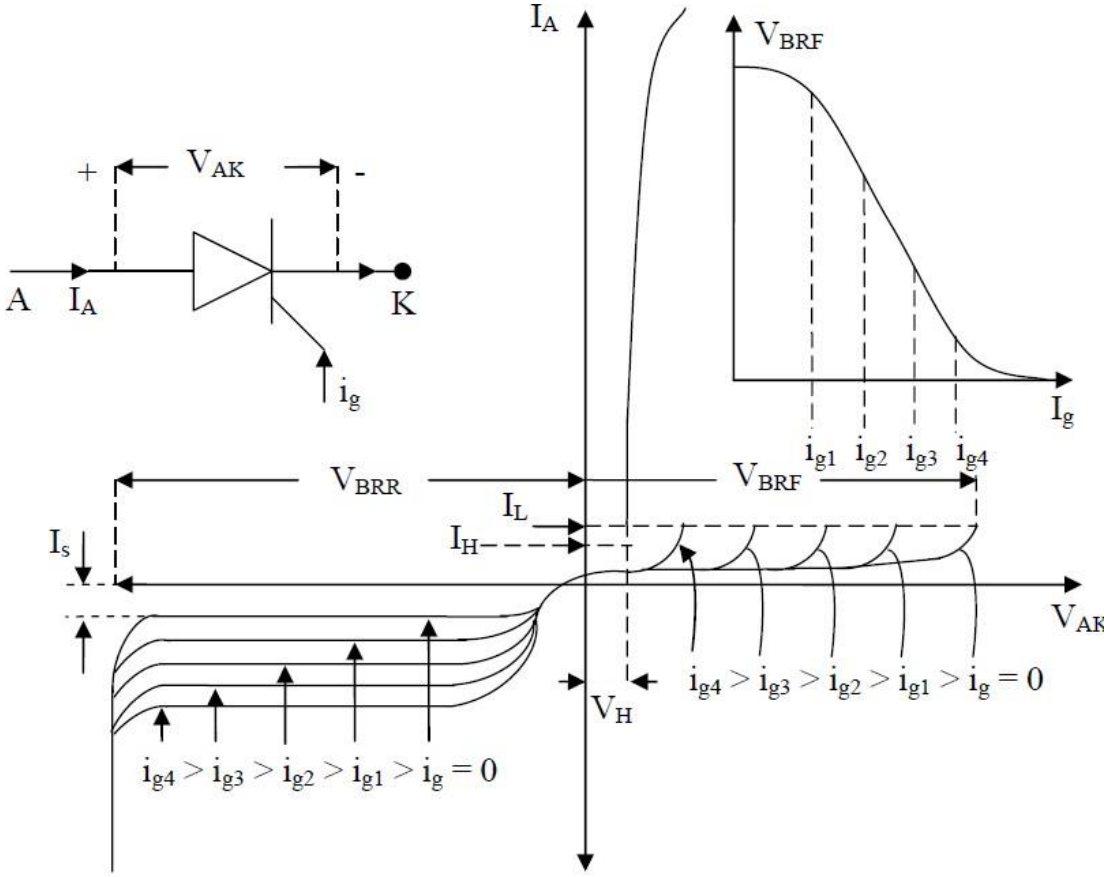


Fig. 4.3: Static output characteristics of a Thyristor

The circuit symbol in the left hand side inset defines the polarity conventions of the variables used in this figure.

With ig = 0, V_{AK} has to increase up to forward break over voltage V_{BRF} before significant anode current starts flowing. However, at V_{BRF} forward break over takes place and the voltage across the thyristor drops to V_H (holding voltage). Beyond this point voltage across the thyristor (V_{AK}) remains almost constant at V_H (1-1.5v) while the anode current is determined by the external load.

The magnitude of gate current has a very strong effect on the value of the break over voltage as shown in the figure. The right hand side figure in the inset shows a typical plot of the forward break over voltage (V_{BRF}) as a function of the gate current (I_g)

After ‑Turn ON‖ the thyristor is no more affected by the gate current. Hence, any current pulse (of required magnitude) which is longer than the minimum needed for ‑Turn ON‖ is sufficient to effect control. The minimum gate pulse width is decided by the external

circuit and should be long enough to allow the anode current to rise above the latching current (I_L) level.

The left hand side of Fig 4.3 shows the reverse i-v characteristics of the thyristor. Once the thyristor is ON the only way to turn it OFF is by bringing the thyristor current below holding current (I_H). The gate terminal has no control over the turn OFF process. In ac circuits with resistive load this happens automatically during negative zero crossing of the supply voltage. This is called –natural commutation‖ or –line commutation‖. However, in dc circuits some arrangement has to be made to ensure this condition. This process is called –forced commutation.‖

During reverse blocking if $i_g = 0$ then only reverse saturation current (I_s) flows until the reverse voltage reaches reverse break down voltage (V_{BRR}). At this point current starts rising sharply. Large reverse voltage and current generates excessive heat and destroys the device. If $i_g > 0$ during reverse bias condition the reverse saturation current rises as explained in the previous section. This can be avoided by removing the gate current while the thyristor is reverse biased.

The static output i-v characteristics of a thyristor depends strongly on the junction temperature as shown in Fig 4.4.

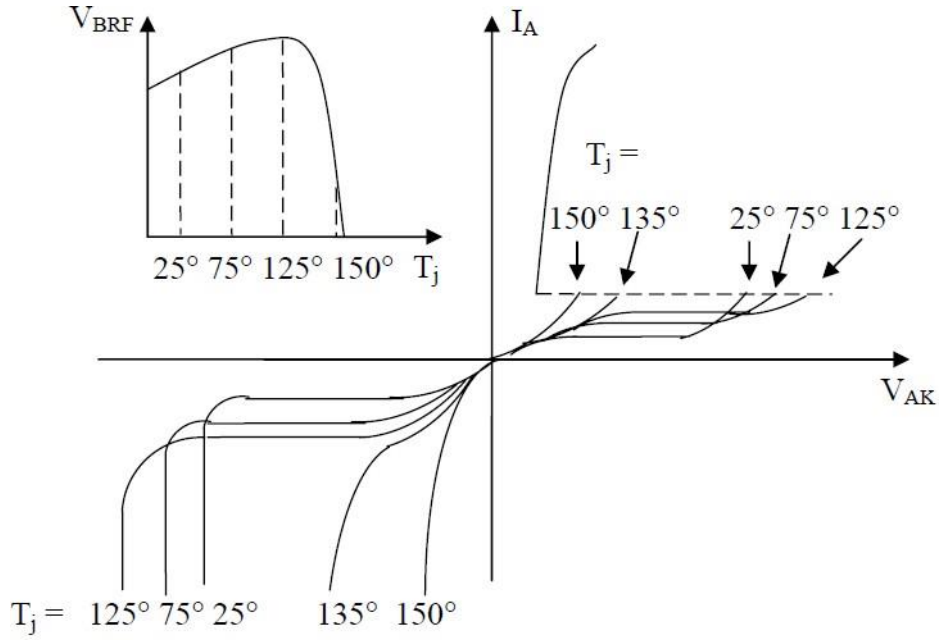


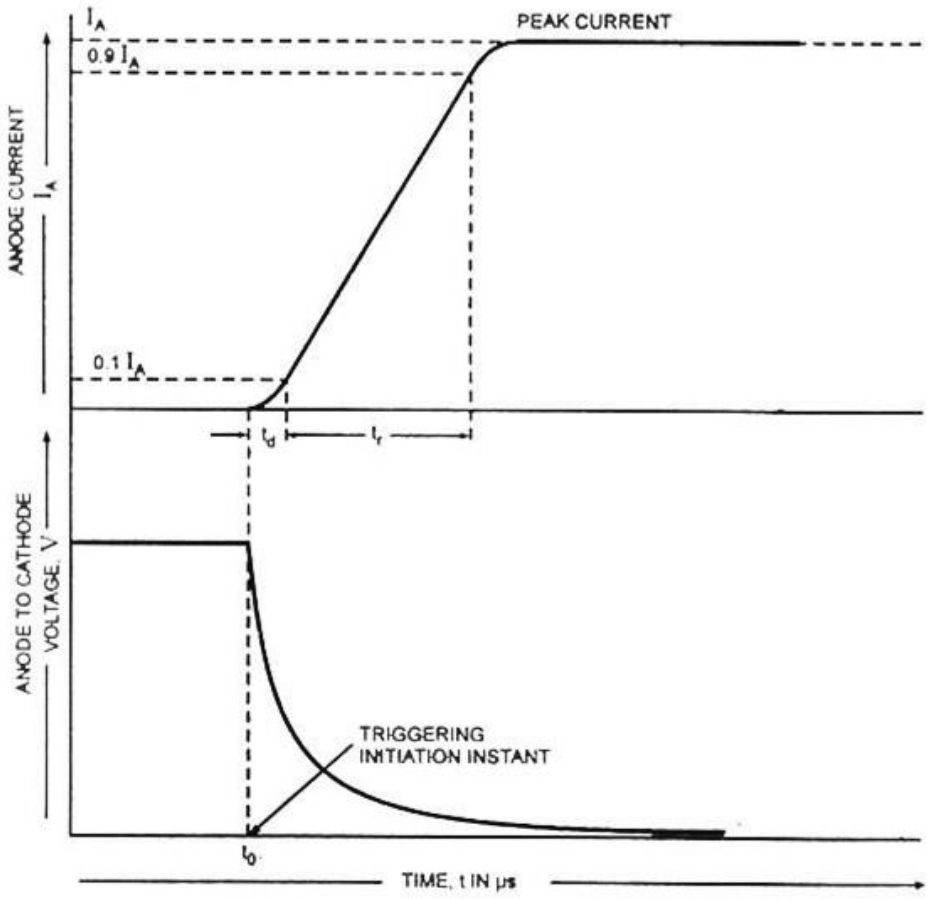
Fig. 4.4: Effect of junction temperature (T_j) on the output i – v characteristics of a thyristor.

Dynamic characteristics

Turn-on and turn-off characteristics of an SCR are called the dynamic characteristics of the SCR.

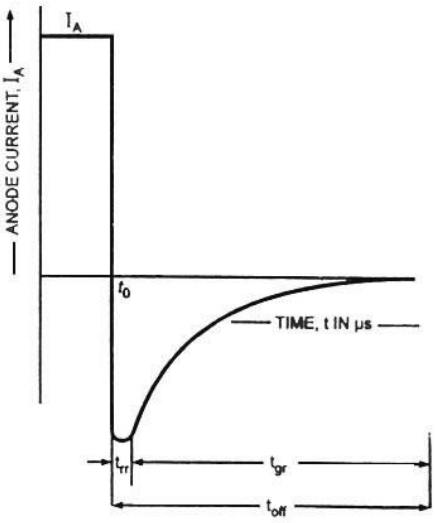
(a) Turn-On Characteristic.

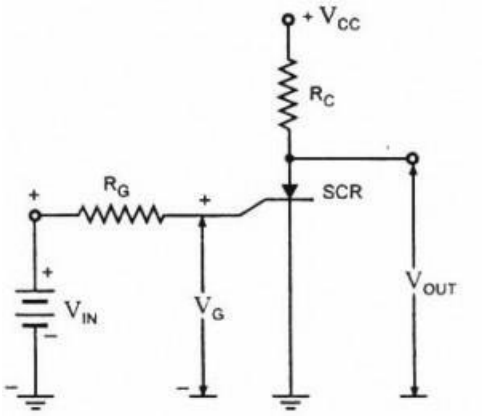
The turn-on time characteristic shows the variation of current and voltage during turn-on. Turn-on time is defined as the time from the initiation of triggering, when the SCR offers infinite impedance to the flow of anode current, to the time when an equilibrium charge distribution is established throughout the device together with a steady state forward voltage drop. The turn-on time is about 1 to 3 micro seconds for the SCR readily available commercially.



The above Figure shows the form of current rise during the transition from the non-conducting to the fully conducting state. The time **t_0** indicate the initiation of turn-on which is caused by a step function of voltage applied to the gate. The period **t_d** is the delay time between the front of the gate pulse and the beginning of a rapid rate of increase of anode current. During the initial interval of turn-on (**t_d**) only a small area near the gate electrode conducts anode current. t_d is due to the charge build up time and decreases with the increase in

gate current. The rise time, t_r depends on the speed at which charges build up to support the final anode current, I_A. t_r is independent of gate current but depends upon the widths of base construction of SCR. The sum of t_d and t_c gives turn-on time t_{on}. The turn-on time i_{on} depends on the anode circuit parameters, gate current amplitude and rise time. The turn-on time is important in pulse triggering.





An SCR Circuit

(b) Turn-off Characteristic.

Turn-off means that all forward conduction has ceased and the re-application of a positive voltage to the anode will not cause flow of current without there being a gate signal. The turn-off characteristic is shown in figure. The time t_0 indicates the instant of application of reverse voltage, t_{rr} is the duration for which the reverse recovery current flows after application of reverse voltage and t is the time required for the recombination of all excess carriers in the inner two layers of the device. The sum of time duration t_{rr} and time duration t gives the turn-off time t_{off}, that is $t_{off} = t_{rr} + t_{gr}$. At the end of turn-off time, a depletion layer gets developed across junction J_2 and now SCR is capable of withstanding forward voltage. The turn-off time depends upon anode current, magnitude of reverse voltage and the rate of application of forward voltage.

1.2.4 Applications of SCR

1. Power Control.

Because of the bistable characteristics of semiconductor devices, whereby they can be switched on and off, and the efficiency of gate control to trigger such devices, the SCRs are ideally suited for many industrial applications. SCRs have got specific advantages over

saturable core reactors and gas tubes owing to their compactness, reliability, low losses, and speedy turn-on and turn-off.

The bistable states (conducting and non-conducting) of the SCR and the property that enables fast transition from one state to the other are made use of in the control of power in both ac and dc circuits.

2. Switching.

Thyristor, being bistable device is widely used for switching of power signals owing to their long life, high operation speed and freedom from other defects associated with mechanical and electro-mechanical switches.

3. Zero Voltage Switching.

In some ac circuits it is necessary to apply the voltage to the load when the instantaneous value of this voltage is going through the zero value. This is to avoid a high rate of increase of current in case of purely resistive loads such as lighting and furnace loads, and thereby reduce the generation of radio noise and hot-spot temperatures in the device carrying the load current.

4. Over-Voltage Protection.

SCRs can be employed for protecting other equipment from over-voltages owing to their fast switching action. The SCR employed for protection is connected in parallel with the load. Whenever the voltage exceeds a specified limit, the gate of the SCR will get energized and trigger the SCR. A large current will be drawn from the supply mains and voltage across the load will be reduced. Two SCRs are used—one for the positive half-cycle and the other for negative half-cycle.

5. Pulse Circuits.

SCRs are used for producing high voltage/current pulses of desired waveform and duration.

6. Battery Charging Regulator.

1.3 DIAC

1.3.1 Operation, construction of DIAC and V-I characteristics curve

A diac is a two-terminal, three layer bidirectional device which can be switched from its OFF state to ON state for either polarity of applied voltage.

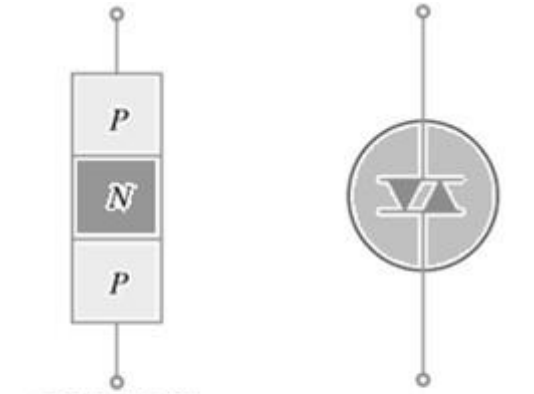
The diac can be constructed in either npn or pnp form. Fig. (i) shows the basic structure of a diac in pnp form. The two leads are connected to p-regions of silicon separated by an n-region. The structure of diac is very much similar to that of a transistor. However, there are several important differences:

(i) There is no terminal attached to the base layer.

(ii) The three regions are nearly identical in size.

(iii) The doping concentrations are identical (unlike a bipolar transistor) to give the device symmetrical properties.

Fig. (ii) shows the symbol of a diac.



DIAC BASIC CONSTRUCTION
(i)

DIAC SYMBOL
(ii)

Operation

When a positive or negative voltage is applied across the terminals of a diac, only a small leakage current IBO will flow through the device. As the applied voltage is increased, the leakage current will continue to flow until the voltage reaches the breakover voltage VBO. At this point, avalanche breakdown of the reverse-biased junction occurs and the device exhibits negative resistance i.e. current through the device increases with the decreasing values of applied voltage. The voltage across the device then drops to _breakback' voltage VW. Fig (iii) shows the V-I characteristics of a diac. For applied positive voltage less than + VBO and negative voltage less than − VBO, a small leakage current (± IBO) flows through the device. Under such conditions, the diac blocks the flow of current and effectively behaves

as an open circuit. The voltages + VBO and − VBO are the breakdown voltages and usually have a range of 30 to 50 volts.

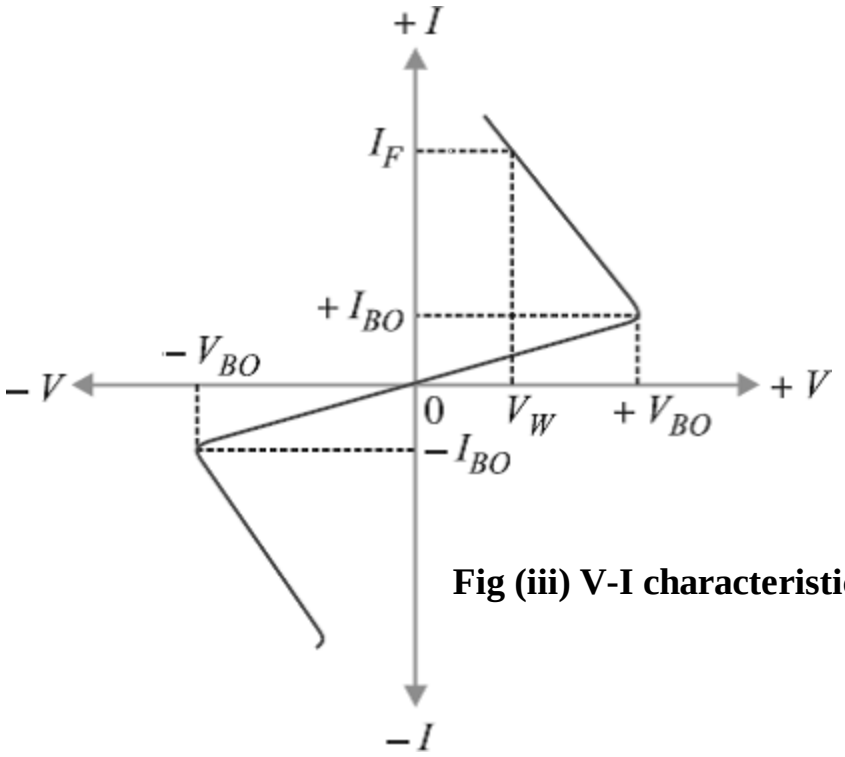


Fig (iii) V-I characteristics of a diac

When the positive or negative applied voltage is equal to or greater than the breakdown voltage, diac begins to conduct and the voltage drop across it becomes a few volts. Conduction then continues until the device current drops below its holding current. Note that the breakover voltage and holding current values are identical for the forward and reverse regions of operation. The DIAC can be used in many applications such as motor speed controls and light dimmers circuit.

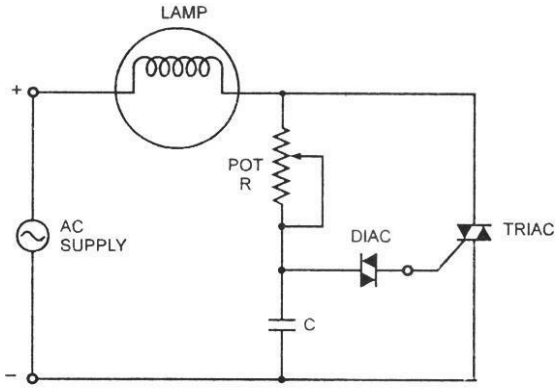
1.3.2 Applications of DIAC

The **diacs**, because of their symmetrical bidirectional switching characteristics, are widely used as triggering devices in triac phase control circuits employed for lamp dimmer, heat control, universal motor speed control etc.

Although a **triac** may be fired into the conducting state by a simple resistive triggering circuit, but triggering devices are typically placed in series with the gates of SCRs and triacs as they give reliable and fast triggering. Diac is the most popular triggering device for the triac. This is illustrated in the following applications.

1. Triac Lamp Dimmer Circuit.

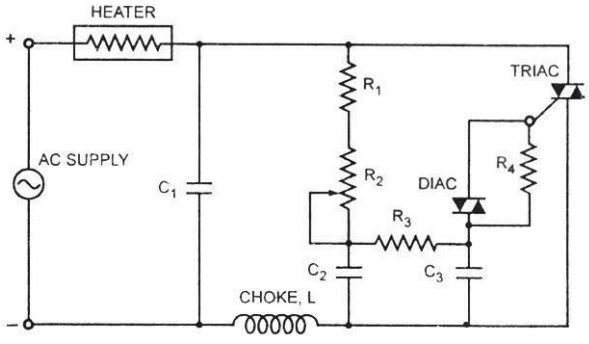
The circuit for a triac controlled by an R-C phase-shift network and a diac is given in figure. This circuit is an example of a simple lamp dimmer. The triac conduction angle is adjusted by adjusting the potentiometer R. The longer the triac conducts, the brighter the lamp will be. The diac acts like an open-circuit until the voltage across the capacitor exceeds its breakover or switching voltage (and the triac's required gate trigger voltage).



Triac Lamp Dimmer Circuit

2. Heat Control Circuit.

A typical diac-triac circuit used for smooth control of ac power to a heater is shown in figure. The capacitor C_1 in series with choke L across the triac slows-up the voltage rise across the device during off-state. The resistor R_4 across the diac ensures smooth control at all positions of potentiometer R_2. The triac conduction angle is adjusted by adjusting the potentiometer R_2. The longer the triac conducts, the larger the output will be from the heater. Thus a smooth control of the heat output from the heater is obtained.



(Heat Control Circuit using Diac)

1.4 TRIAC

1.4.1 Operation, construction of TRIAC and V-I characteristics curve

The Triac is a member of the thyristor family. But unlike a thyristor which conducts only in one direction (from anode to cathode) a triac can conduct in both directions. Thus a triac is similar to two back to back (anti parallel) connected thyristosr but with only three terminals.

Construction and operating principle

Fig. 5 (a) and (b) show the circuit symbol and schematic cross section of a triac respective. As the Triac can conduct in both the directions the terms –anode‖ and –cathode‖ are not used for Triacs. The three terminals are marked as MT_1 (Main Terminal 1), MT_2 (Main Terminal 2) and the gate by G. As shown in Fig 5 (b) the gate terminal is near MT_1 and is connected to both

N_3 and P_2 regions by metallic contact. Similarly MT_1 is connected to N_2 and P_2 regions while MT_2 is connected to N_4 and P_1 regions.

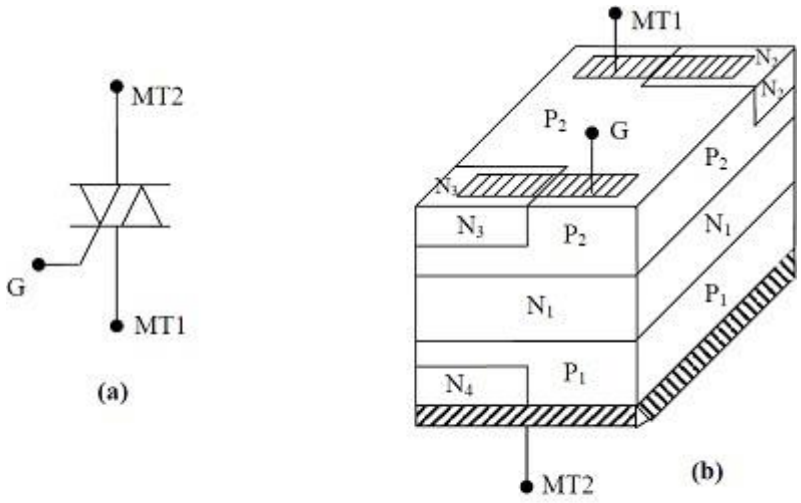


Fig.5 Circuit symbol and schematic construction of a Triac
(a) Circuit symbol (b) Schematic construction.

V-I characteristics

From a functional point of view a triac is similar to two thyristors connected in anti parallel. Therefore, it is expected that the V-I characteristics of Triac in the 1^{st} and 3^{rd} quadrant of the V-I plane will be similar to the forward characteristics of a thyristors. As shown in Fig. 6, with no signal to the gate the triac will block both half cycle of the applied ac voltage provided its peak value is lower than the break over voltage (V_{BO}) of the device. However, the turning on of the triac can be controlled by applying the gate trigger pulse at the desired

instance. Mode-1 triggering is used in the first quadrant where as Mode-3 triggering is used in the third quadrant.

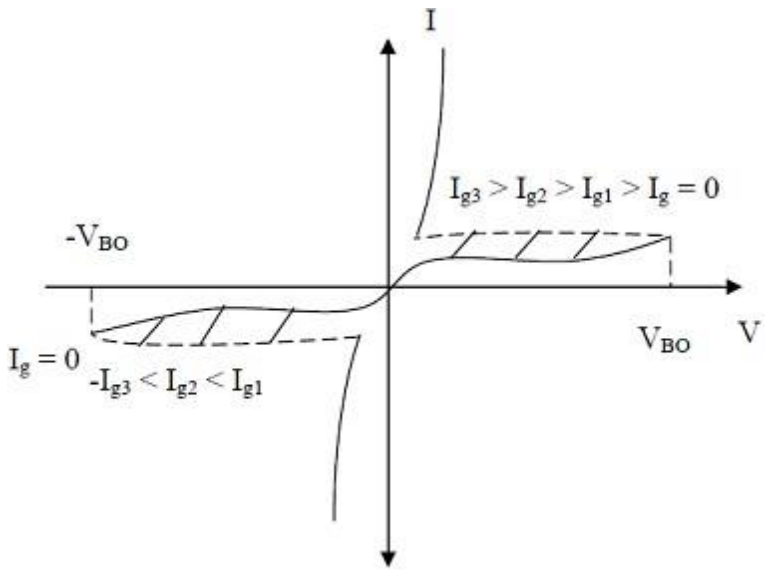


Fig. 6 : Steady state V – I characteristics of a Triac

As such, most of the thyristor characteristics apply to the triac (ie, latching and holding current). However, in a triac the two conducting paths (from MT_1 to MT_2 or from MT_1 to MT_1) interact with each other in the structure of the triac. Therefore, the voltage, current and frequency ratings of triacs are considerably lower than thyristors. At present triacs with voltage and current ratings of 1200V and 300A (rms) are available. Triacs also have a larger on state voltage drop compared to a thyristor.

1.4.2 Modes of operation of TRIAC and mention the preferred modes

Since a Triac is a bidirectional device and can have its terminals at various combinations of positive and negative voltages, there are four possible electrode potential combinations as given below

1. MT_2 positive with respect to MT_1, G positive with respect to MT_1
2. MT_2 positive with respect to MT_1, G negative with respect to MT_1
3. MT_2 negative with respect to MT_1, G negative with respect to MT_1
4. MT_2 negative with respect to MT_1, G positive with respect to MT_1

The triggering sensitivity is highest with the combinations 1 and 3 and are generally used. However, for bidirectional control and uniforms gate trigger mode sometimes trigger

modes 2 and 3 are used. Trigger mode 4 is usually avoided. Fig 7 (a) and (b) explain the conduction mechanism of a triac in trigger modes 1 & 3 respectively.

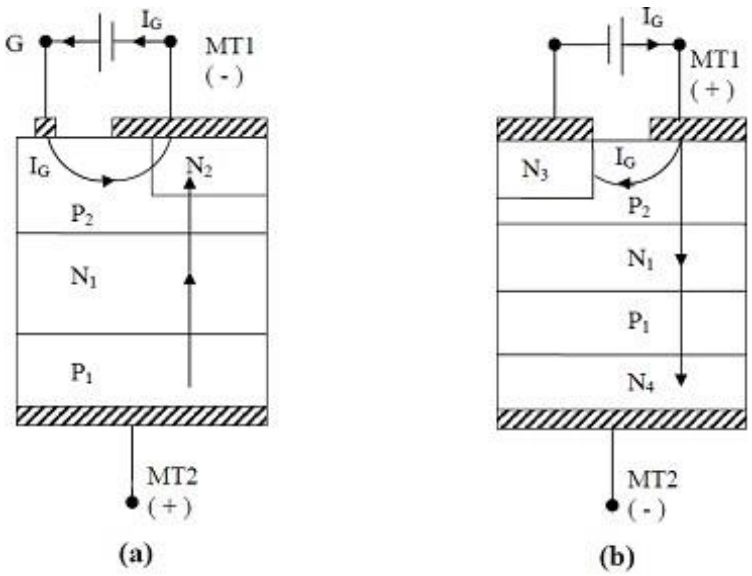


Fig. 7 Conduction mechanism of a triac in trigger modes 1 and 3
(a) Mode – 1 , (b) Mode – 3 .

In trigger mode-1 the gate current flows mainly through the P_2 N_2 junction like an ordinary thyristor. When the gate current has injected sufficient charge into P_2 layer the triac starts conducting through the P_1 N_1 P_2 N_2 layers like an ordinary thyristor.

In the trigger mode-3 the gate current I_g forward biases the P_2 P_3 junction and a large number of electrons are introduced in the P_2 region by N_3. Finally the structure P_2 N_1 P_1 N_4 turns on completely.

1.4.3 Applications of TRIAC (Phase control using TRIAC)

A triac is functionally equivalent to two anti parallel connected thyristors. It can block voltages in both directions and conduct current in both directions.

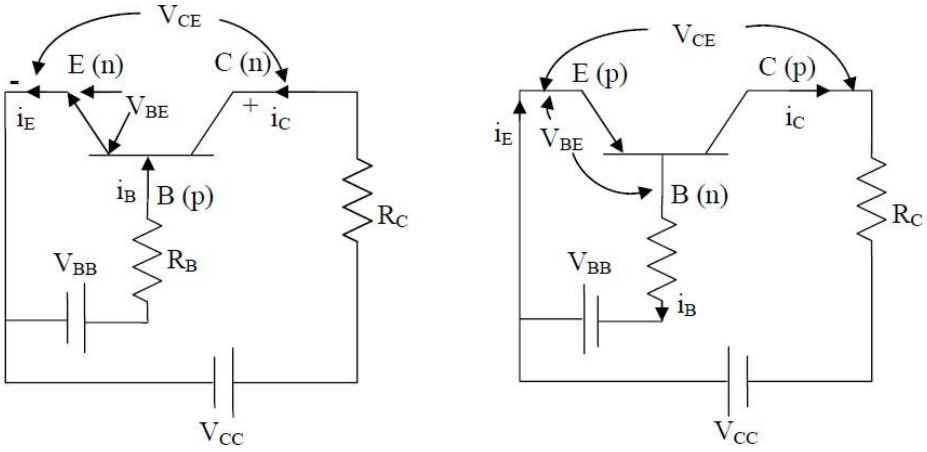
• A triac has three terminals like a thyristor. It can be turned on in either half cycle by either a positive on a negative current pulse at the gate terminal.

• Triacs are extensively used at power frequency ac load (eg heater, light, motors) control applications.

1.5 Power BJT

1.5.1 Operation, construction of an NPN POWER Transistor as a switch

Power Bipolar Junction Transistor (BJT) is the first semiconductor device to allow full control over its Turn on and Turn off operations. It simplified the design of a large number of Power Electronic circuits that used forced commutated thyristors at that time and also helped realize a number of new circuits. BJT was the first semiconductor device to closely approximate an ideal fully controlled Power switch.



A junction transistor consists of a semiconductor crystal in which a **p** type region is sandwiched between two **n** type regions. This is called an **n-p-n** transistor. Alternatively an **n** type region may be placed in between two **p** type regions to give a **p-n-p** transistor. Fig above shows the circuit symbols and schematic representations of an **n-p-n** and a **p-n-p** transistor. The terminals of a transistor are called Emitter (E), Base (B) & Collector (C) as shown in the figure.

When a transistor is used as a controlled switch, the control current input is provided at the base terminal. The control circuit is connected between the base and emitter. The power terminals of the switch are the collector and the emitter.

The output characteristic is a plot of the current ***Ic*** through the switch

versus the voltage VCE across it for a fixed value of the current I□ .

Let us assume that V = 150 V, R = 30Ω and decide to keep I□ at 0.6A. The voltage VCE across the switch and the current ***Ic*** through it must be given by a point on the characteristic for I□ = 0.6 A. To locate this point, we used a second relationship by a straight line called the "load line."

$$V_{CE} = V - I_C R = 150V - I_C \cdot 30\Omega$$

What will happen if we progressively reduce the base current I_B.

IB	IC	VCE	PDIS=VCE IC
0.6 A	≈5A	VCE(SAT)≈2.5V	12.5W
0.4 A	≈5A	VCE(SAT)≈2.5V	12.5W
0.2 A	3A	60 V	180W

For I_B = 0.2 A, the intersection point gives VCE = 60 V and a current of 3 A. The transistor is no longer in the saturated ON state. Such a condition is to be avoided, because, there is excessive power dissipation in the transistor (180W), which can result in its damage.

It is necessary to ensure a saturated ON state, by providing adequate base drive current, for the safe and satisfactory operation of the switch. Therefore, the minimum base current to ensure the saturated ON state is given by IB=IC/hFE where hFE is a parameter specified in the data sheet of the transistor.

Often it will be advisable to use a somewhat higher value of base current than that indicated by the above formula, as a safety feature, to take care of possible increases in ***Ic*** above the anticipated value.

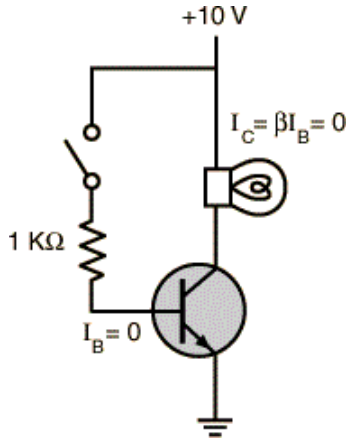
1.5.2 Applications of BJT in Power switching applications

There are two types of **applications of BJT**, switching and amplification.

Transistor as a Switch

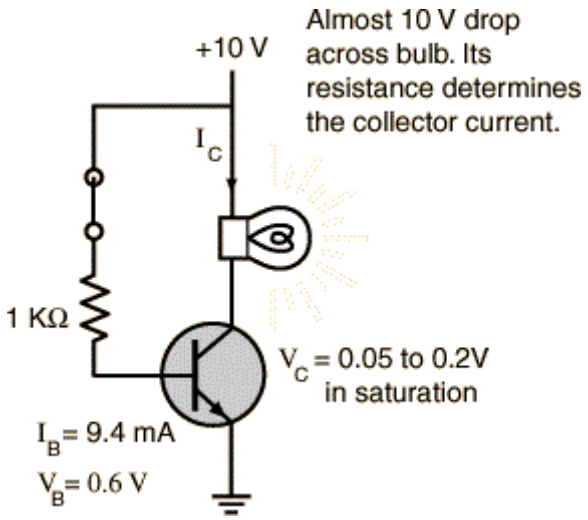
For switching applications transistor is biased to operate in the saturation or cutoff region. Transistor in cutoff region will act as an open switching whereas in saturation will act as a closed switch.

Open Switch



In the cutoff region (both junctions are reversed biased) the voltage across the CE junction is very high. The input voltage is zero so both base and collector currents are zero, hence the resistance offered by the BJT is very high (ideally infinite).

Closed Switch



In saturation (both junctions are forward biased) a high input voltage is applied to the base. The value of base resistance is adjusted such that a large base current flows. There is a small voltage drop across the collector emitter junction of the order of 0.05 to 0.2V and collector current is very large. A very small voltage drop takes place across the BJT and it can be said to be equivalent to a closed switch.

1.6 Power MOSFET

1.6.1 Operation, construction of Power MOSFET & its characteristics curve

Power MOSFET is a device that evolved from MOS integrated circuit technology. The first attempts to develop high voltage MOSFETs were by redesigning lateral MOSFET to increase their voltage blocking capacity.

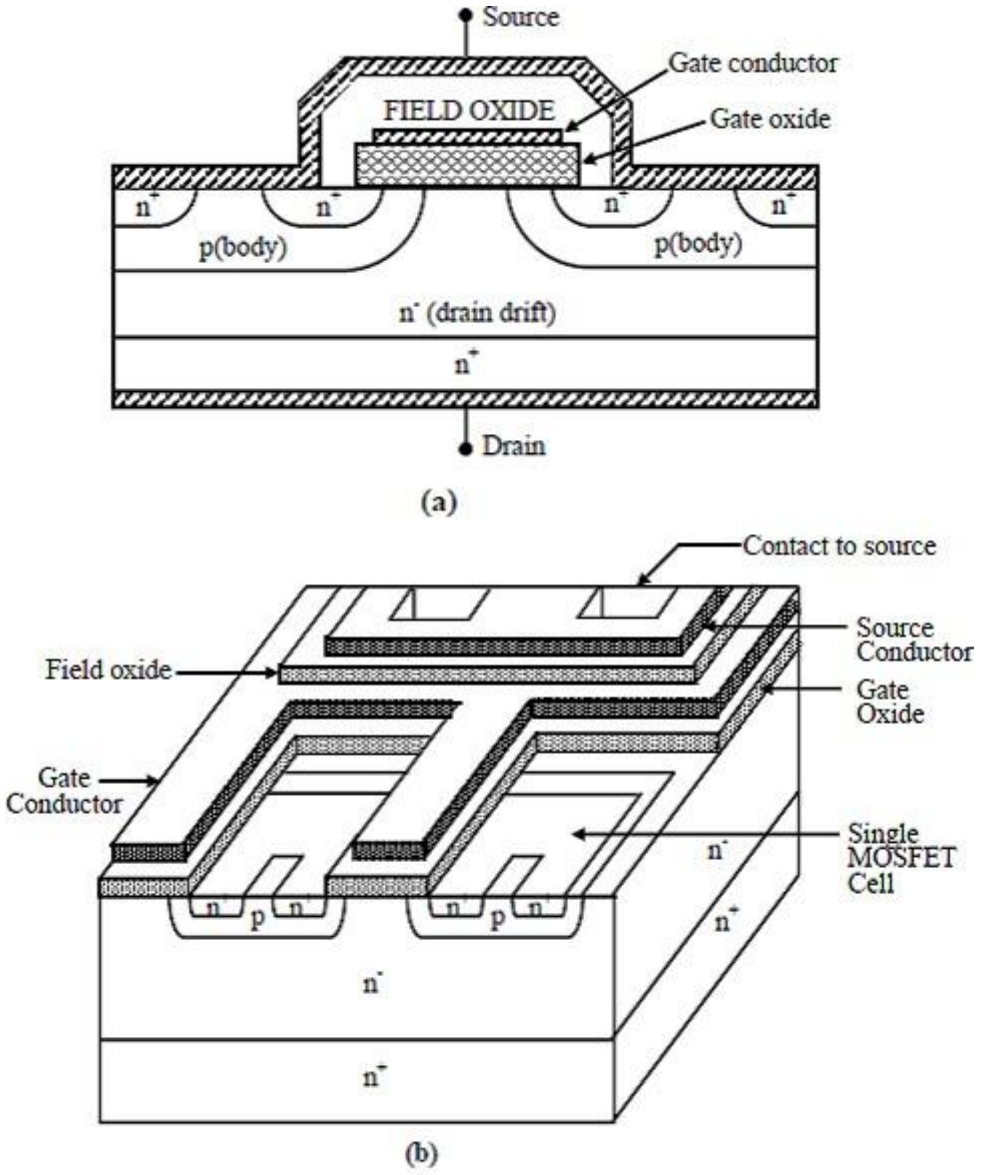


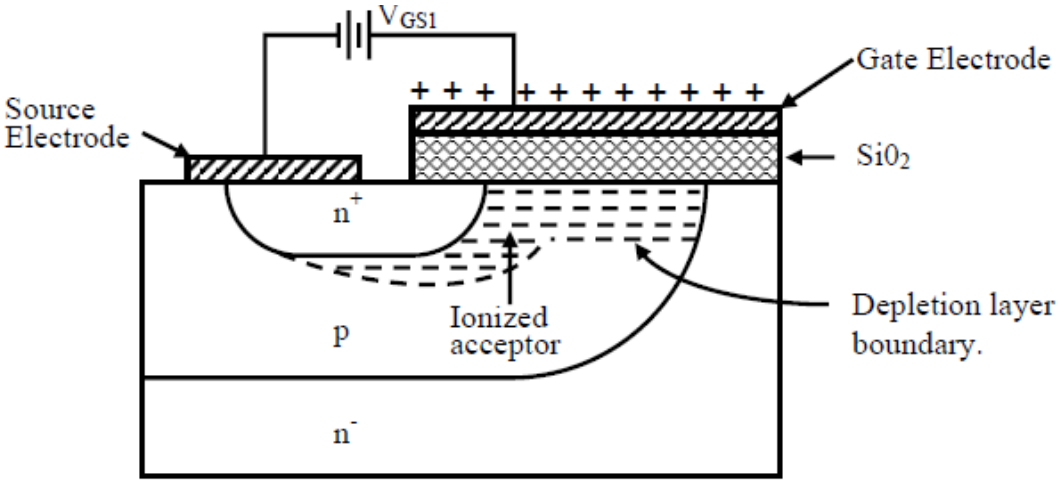
Fig. 8 Schematic construction of a power MOSFET
(a) Construction of a single cell.
(b) Arrangement of cells in a device.

The resulting technology was called lateral double deffused MOS (DMOS). However it was soon realized that much larger breakdown voltage and current ratings could be achieved by resorting to a vertically oriented structure. Since then, vertical DMOS (VDMOS) structure has been adapted by virtually all manufacturers of Power MOSFET. A power MOSFET using

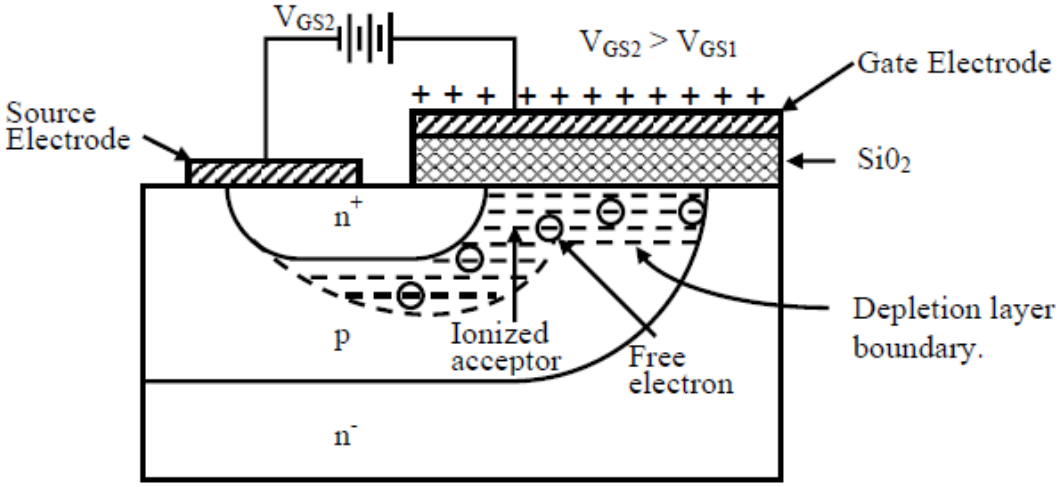
VDMOS technology has vertically oriented three layer structure of alternating **p** type and **n** type semiconductors as shown in Fig 8 (a) which is the schematic representation of a single MOSFET cell structure. A large number of such cells are connected in parallel (as shown in Fig 8 (b)) to form a complete device

Operation

The gate region of a MOSFET which is composed of the gate metallization, the gate (silicon) oxide layer and the p-body silicon forms a high quality capacitor. When a small voltage is application to this capacitor structure with gate terminal positive with respect to the source (note that body and source are shorted) a depletion region forms at the interface between the SiO_2 and the silicon as shown in Fig 9 (a).



(a)



(b)

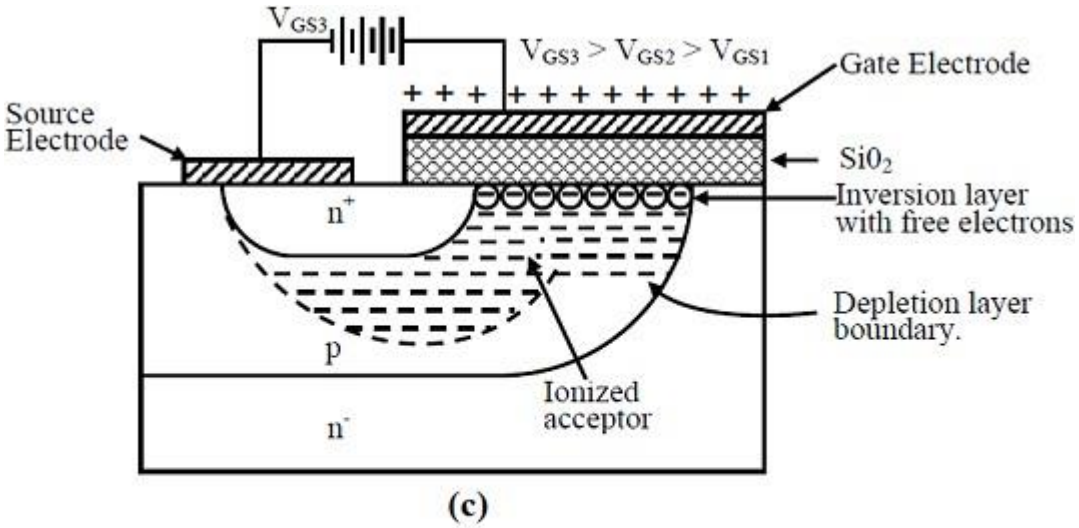


Fig. 9 Gate control of MOSFET conduction.
(a) Depletion layer formation;
(b) Free electron accumulation;
(c) Formation of inversion layer.

The positive charge induced on the gate metallization repels the majority hole carriers from the interface region between the gate oxide and the **p** type body. This exposes the negatively charged acceptors and a depletion region is created.

Further increase in V_{GS} causes the depletion layer to grow in thickness. At the same time the electric field at the oxide-silicon interface gets larger and begins to attract free electrons as shown in Fig 9 (b). The immediate source of electron is electron-hole generation by thermal ionization. The holes are repelled into the semiconductor bulk ahead of the depletion region. The extra holes are neutralized by electrons from the source.

As V_{GS} increases further the density of free electrons at the interface becomes equal to the free hole density in the bulk of the body region beyond the depletion layer. The layer of free electrons at the interface is called the inversion layer and is shown in Fig 9 (c). The inversion layer has all the properties of an **n** type semiconductor and is a conductive path or ‑channel‖ between the drain and the source which permits flow of current between the drain and the source. Since current conduction in this device takes place through an **n**- type ‑channel‖ created by the electric field due to gate source voltage it is called ‑Enhancement type n-channel MOSFET‖.

The value of V_{GS} at which the inversion layer is considered to have formed is called the ‑Gate – Source threshold voltage V_{GS} (th)‖. As V_{GS} is increased beyond V_{GS}(th) the inversion layer gets somewhat thicker and more conductive, since the density of free electrons

increases further with increase in V_{GS}. The inversion layer screens the depletion layer adjacent to it from increasing V_{GS}. The depletion layer thickness now remains constant.

Steady state output i-v characteristics of a MOSFET

The MOSFET, like the BJT is a three terminal device where the voltage on the gate terminal controls the flow of current between the output terminals, Source and Drain. The source terminal is common between the input and the output of a MOSFET. The output characteristics of a MOSFET is then a plot of drain current (i_D) as a function of the Drain – Source voltage (v_{DS}) with gate source voltage (v_{GS}) as a parameter. Fig 10 (a) shows such a characteristics.

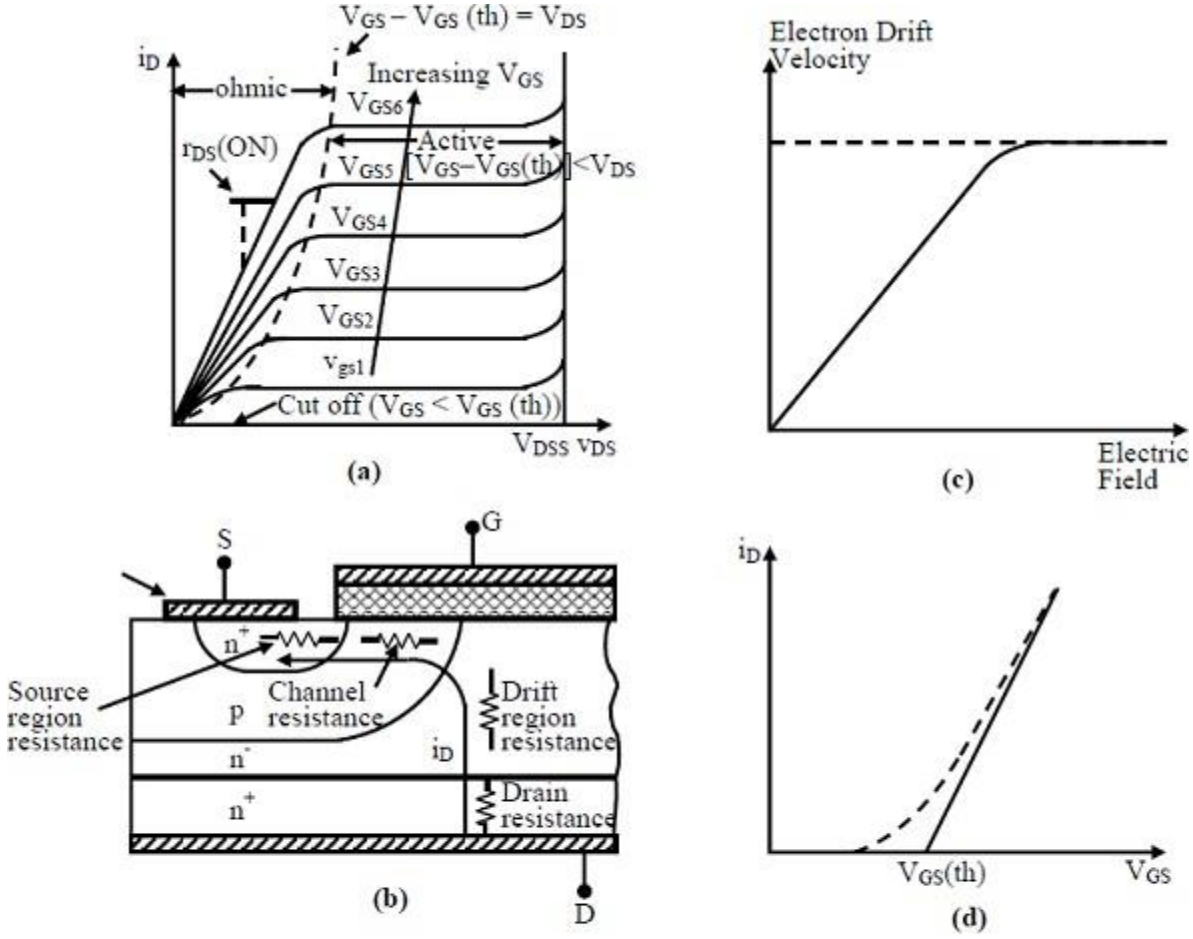


Fig. 10 Output i-v characteristics of a Power MOSFET
(a) i-v characteristics;
(b) Components of ON-state resistance;
(c) Electron drift velocity vs Electric field;
(d) Transfer

With gate-source voltage (V_{GS}) below the threshold voltage (v_{GS} (th)) the MOSFET operates in the cut-off mode. No drain current flows in this mode and the applied drain–source voltage (v_{DS}) is supported by the body-collector **p-n** junction. Therefore, the maximum applied voltage should be below the avalanche break down voltage of this junction (V_{DSS}) to avoid destruction of the device.

When V_{GS} is increased beyond v_{GS}(th) drain current starts flowing. For small values of v_{DS} ($v_{DS} < (v_{GS} - v_{GS}(th))$ i_D is almost proportional to v_{DS}. Consequently this mode of operation is called ‑ohmic mode‖ of operation. In power electronic applications a MOSFET is operated either in the cut off or in the ohmic mode. The slope of the $v_{DS} - i_D$ characteristics in this mode is called the ON state resistance of the MOSFET (r_{DS} (ON)). Several physical resistances as shown in Fig 10 (b) contribute to r_{DS} (ON). Note that r_{DS} (ON) reduces with increase in v_{GS}. This is mainly due to reduction of the channel resistance at higher value of

v_{GS}. Hence, it is desirable in power electronic applications, to use as large a gate-source voltage as possible subject to the dielectric break down limit of the gate-oxide layer.

1.6.2 Applications of MOSFET

1 MOSFET as an analog switch

Enhancement mode MOSFET based analog switches use the transistor channel as a low resistance to pass analog signals when on, and as a high impedance when off. Signals can flow in either direction across a MOSFET switch. In this application the drain and source of a MOSFET exchange places depending on the voltages of each electrode compared to that of the gate and the direction of current flow. For a simple MOSFET without an integrated diode from source to drain (or the back gate or body terminal tied to the source), the source is the more negative side for an NMOS or the more positive side for a PMOS. All of these switches are limited as to what signals they can pass when on or block when off by their gate-source, gate-drain and source-drain voltages, and source-to-drain currents; exceeding these voltage or current limits will potentially damage the switch.

2 Switched Capacitor Circuits

A switched capacitor is an electronic circuit element used in discrete time signal processing systems. It works by transferring charge into and out of a capacitor when switches are opened and closed. Usually, non-overlapping signals are used to control the switches, often termed Break before Make switching, so that all switches are open for a very short time during the switching transitions. Discrete time filters implemented with these elements are termed 'switched-capacitor filters'. Unlike continuous time analog filters, which must be constructed with resistors, capacitors and sometimes inductors whose values are accurately known, switched capacitor filters depend only on the ratios between capacitances and the switching frequency. This makes them much more suitable for use within integrated circuits, where the accurately specified absolute value of components such as resistors and capacitors are not economical to construct.

1.7 GTO

1.7.1 Construction, operation of GTO and V-I characteristics

Construction

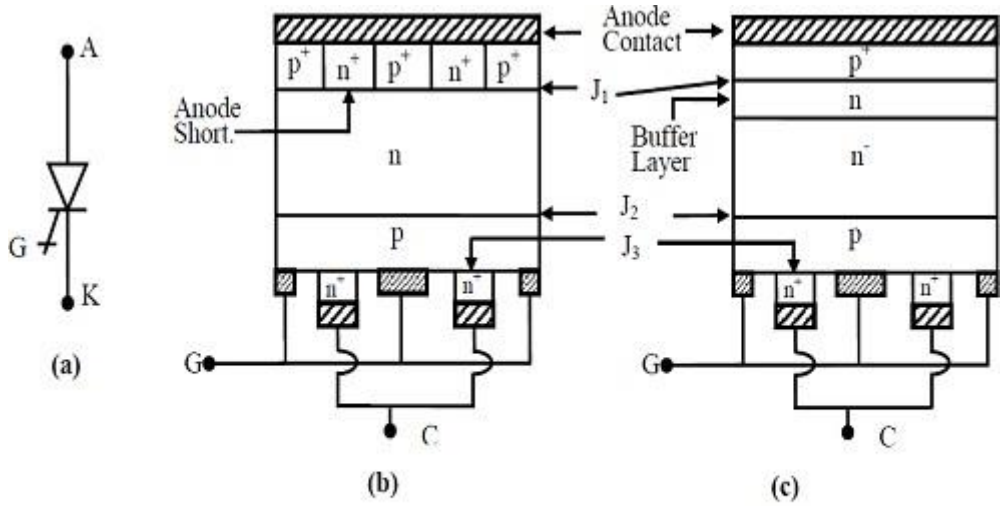


Fig. 11 Circuit symbol and schematic cross section of a GTO (a) Circuit Symbol, (b) Anode shorted GTO structure, (c) Buffer layer GTO structure.

Like a thyristor, a GTO is also a four layer three junction **p-n-p-n** device. In order to obtain high emitter efficiency at the cathode end, the $\mathbf{n}^{+}$ cathode layer is highly doped. Consequently, the break down voltage of the function J_3 is low (typically 20-40V). The **p** type gate region has conflicting doping requirement. To maintain good emitter efficiency the doping level of this layer should be low, on the other hand, from the point of view of good turn off properties, resistively of this layer should be as low as possible requiring the doping level of this region to be high. Therefore, the doping level of this layer is highly graded. Additionally, in order to optimize current turn off capability, the gate cathode junction must be highly interdigitated. A 3000 Amp GTO may be composed of upto 3000 individual cathode segments which are a accessed via a common contact. The most popular design features multiple segments arranged in concentric rings around the device center.

The maximum forward blocking voltage of the device is determined by the doping level and the thickness of the **n** type base region next. In order to block several kv of forward voltage the doping level of this layer is kept relatively low while its thickness is made considerably higher (a few hundred microns). Byond the maximum allowable forward voltage either the electric field at the main junction (J_2) exceeds a critical value (avalanche break

down) or the **n** base fully depletes, allowing its electric field to touch the anode emitter (punch through).

The junction between the **n** base and **p+** anode (J_1) is called the ‑anode junction‖. For good turn on properties the efficiency of this anode junction should be as high as possible requiring a heavily doped **p+** anode region. However, turn off capability of such a GTO will be poor with very low maximum turn off current and high losses. There are two basic approaches to solve this problem.

In the first method, heavily doped **n+** layers are introduced into the **p+** anode layer. They make contact with the same anode metallic contact. Therefore, electrons traveling through the base can directly reach the anode metal contact without causing hole injection from the **p+** anode. This is the classic ‑anode shorted GTO structure‖ as shown in Fig 11 (b). Due to presence of these ‑anode shorts‖ the reverse voltage blocking capacity of GTO reduces to the reverse break down

Voltage of junction J_3 (20-40 volts maximum). In addition a large number of ‑anode shorts‖ reduces the efficiency of the anode junction and degrades the turn on performance of the device. Therefore, the density of the ‑anode shorts‖ are to be chosen by a careful compromise between the turn on and turn off performance.

Operating principle of a GTO

GTO being a monolithic **p-n-p-n** structure just like a thryistor its basic operating principle can be explained in a manner similar to that of a thyristor. In particular, the **p-n-p-n** structure of a GTO can be thought of consisting of one **p-n-p** and one **n-p-n** transistor connected in the regenerative configuration as shown in Fig 12.

From the ‑two transistor analogy‖ (Fig 12 (a)) of the GTO structure one can write.

$$i_{C1} = \alpha_p I_A + I_{CBO1} \qquad (5.1)$$

$$i_{B1} = i_{C2} = \alpha_n I_k + I_{CBO2} \qquad (5.2)$$

$$I_k = I_A + I_G \quad \text{and} \quad I_A = i_{B1} + i_{C1} \qquad (5.3)$$

$$I_A = \frac{\alpha_n I_G + (i_{CBO1} + i_{CBO2})}{1 - (\alpha_n + \alpha_p)} \qquad (5.4)$$

With applied forward voltage V_{AK} less than the forward break over voltage both I_{CBO1} and I_{CBO2} are small. Further if I_G is zero I_A is only slightly higher than ($I_{CBO1} + I_{CBO2}$). Under this condition both α_n and α_p are small and $(\alpha_p + \alpha_n) << 1$. The device is said to be in the forward blocking mode.

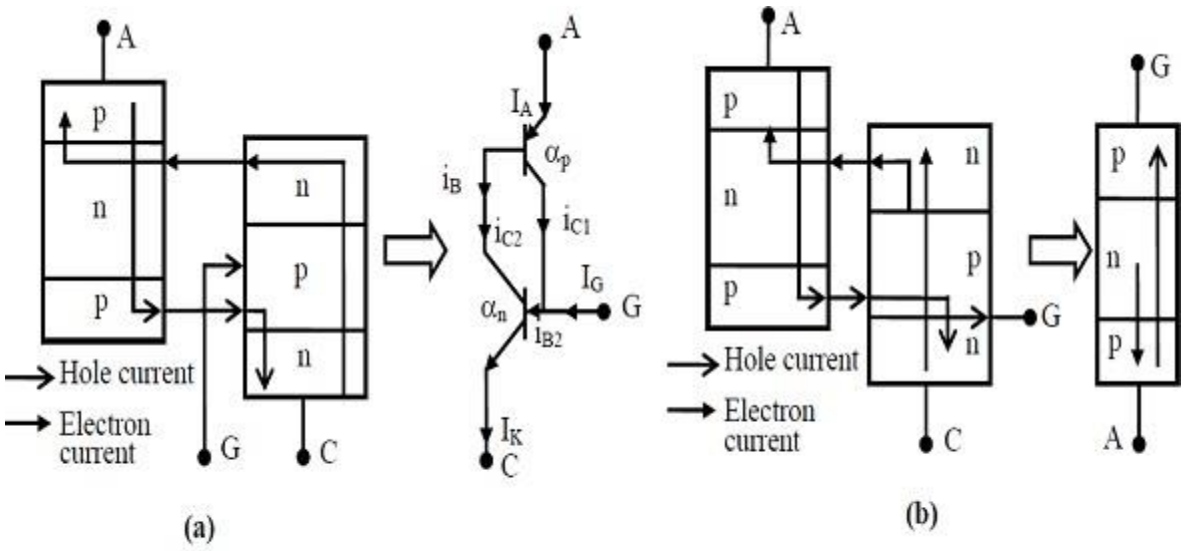


Fig12 Current distribution in a GTO
(a) During turn on; (b) During turn off.

To turn the device on either the anode voltage can be raised until I_{CBO1} and I_{CBO2} increases by avalanche multiplication process or by injecting a gate current. The current gain α of silicon transistors rises rapidly as the emitter current increases. Therefore, any mechanism which causes a momentary increase in the emitter current can be used to turn on the device. Normally, this is done by injecting current into the p base region via the external gate contract. As $\alpha_n + \alpha_p$ approaches unity the anode current tends to infinity. Physically as $\alpha_n + \alpha_p$ nears unity the device starts to regenerate and each transistor drives its companion into saturation. Once in saturation, all junctions assume a forward bias and total potential drop across the device becomes approximately equal to that of a single **p-n** diode. The anode current is restricted only by the external circuit. Once the device has been turned on in this manner, the external gate current is no longer required to maintain conduction, since the regeneration process is self-sustaining. Reversion to the blocking mode occurs only when the anode current is brought below the ‑holding current‖ level.

To turn off a conducting GTO the gate terminal is biased negative with respect to the cathode. The holes injected from the anode are, therefore, extracted from the p base through the gate metallization into the gate terminal (Fig 12 (b)). The resultant voltage drop in the **p** base above the **n** emitter starts reverse biasing the junction J_3 and electron injection stops here. The process originates at the periphery of the **p** base and the **n** emitter segments and the area still injecting electron shrinks. The anode current is crowded into higher and higher density filaments in most remote areas from the gate contact. This is the most critical phase in the GTO turn off process since highly localized high temperature regions can cause device failure unless these current filaments are quickly extinguished. When the last filament disappears, electron injection stops completely and depletion layer starts to grow on both J_2 and J_3. At this point the device once again starts blocking forward voltage. However, although the cathode current has ceased the anode to gate current continues to flow (Fig 12 (b)) as the **n** base excess carriers diffuse towards J_1. This ‑tail current‖ then decays exponentially as the **n** base excess carriers reduce by recombination. Once the tail current has completely disappeared does the device regain its steady state blocking characteristics. ‑Anode Shorts‖ (or transparent emitter) helps reduce the tail current faster by providing an alternate path to the **n** base electrons to reach the anode contact without causing appreciable hole injection from anode.

Steady state output and gate characteristics

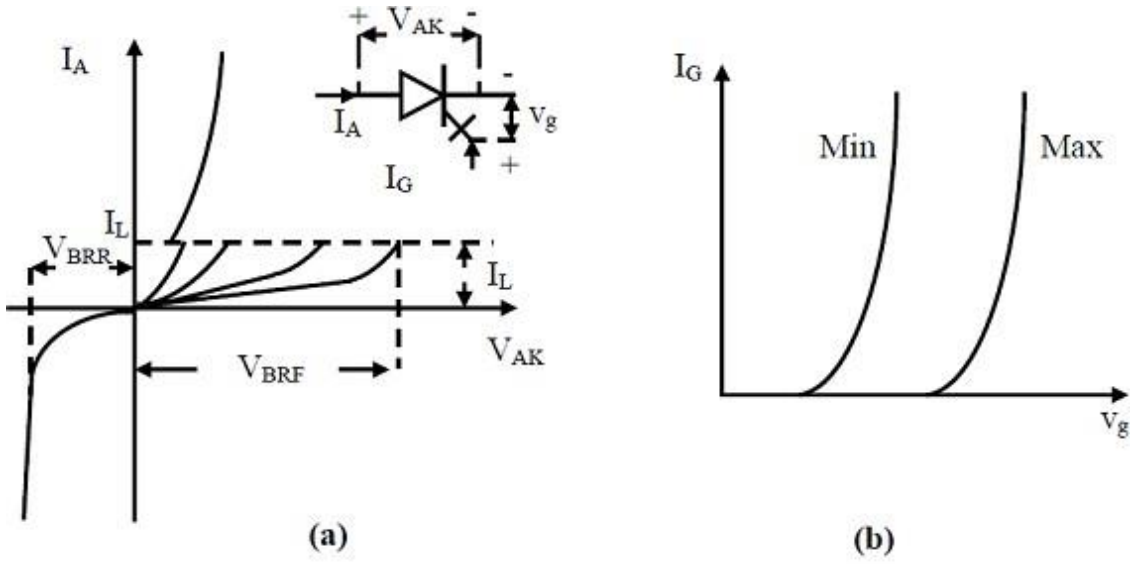


Fig. 13 Steady state characteristics of a GTO
(a) Output characteristics; (b) Gate characteristics.

This characteristic in the first quadrant is very similar to that of a thyristor as shown in Fig. 13 (a). However, the latching current of a GTO is considerably higher than a thyristor of similar rating. The forward leakage current is also considerably higher. In fact, if the gate current is not sufficient to turn on a GTO it operates as a high voltage low gain transistor with considerable anode current. It should be noted that a GTO can block rated forward voltage only when the gate is negatively biased with respect to the cathode during forward blocking state. At least, a low value resistance must be connected across the gate cathode terminal. Increasing the value of this resistance reduces the forward blocking voltage of the GTO. Asymmetric GTOs have small (20-30 V) reverse break down voltage. This may lead the device to operate in ‒reverse avalanche‖ under certain conditions. This condition is not dangerous for the GTO provided the avalanche time and current are small. The gate voltage during this period must remain negative.

Fig 13 (b) shows the gate characteristics of a GTO. The zone between the min and max curves reflects parameter variation between individual GTOs. These characteristics are valid for DC and low frequency AC gate currents.

1.7.2 Application of GTO

The main applications are in variable speed motor drives, high power inverters, static VAR compensators (SVCs) and AC/DC power supplies with high power ratings and traction. GTOs are increasingly being replaced by integrated gate-commutated thyristors, which are an evolutionary development of the GTO, and insulated gate bipolar transistors, which are members of the transistor family.

1.8 IGBT

1.8.1 Operation, construction of IGBT and its characteristics curve

Constructional Features of an IGBT

Vertical cross section of a n channel IGBT cell is shown in Fig 14. Although p channel IGBTs are possible n channel devices are more common

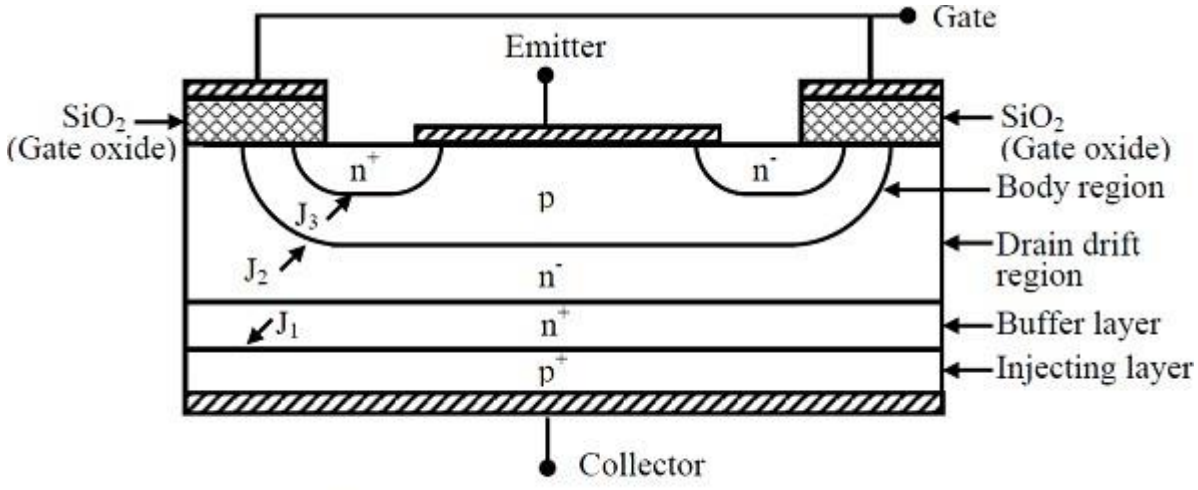


Fig. 14 Vertical cross section of an IGBT cell.

The major difference with the corresponding MOSFET cell structure lies in the addition of a **p+** injecting layer. This layer forms a **pn** junction with the drain layer and injects minority carriers into it. The **n** type drain layer itself may have two different doping levels. The lightly doped **n-** region is called the drain drift region. Doping level and width of this layer sets the forward blocking voltage (determined by the reverse break down voltage of J_2) of the device. However, it does not affect the on state voltage drop of the device due to conductivity modulation as discussed in connection with the power diode. This construction of the device is called ―Punch Through‖ (PT) design. The Non-Punch Through (NPT) construction does not have this added **n+** buffer layer. The PT construction does offer lower on state voltage drop compared to the NPT construction particularly for lower voltage rated devices. However, it does so at the cost of lower reverse break down voltage for the device, since the reverse break down voltage of the junction J_1 is small. The rest of the construction of the device is very similar to that of a **vertical MOSFET** including the insulated gate structure and the shorted body (**p** type) – emitter (**n+** type) structure. The doping level and physical geometry of the **p** type body region however, is considerably different from that of a MOSFET in order to defeat the latch up action of a parasitic thyristor embedded in the IGBT

structure. A large number of basic cells as shown in Fig 14 are grown on a single silicon wafer and connected in parallel to form a complete IGBT device.

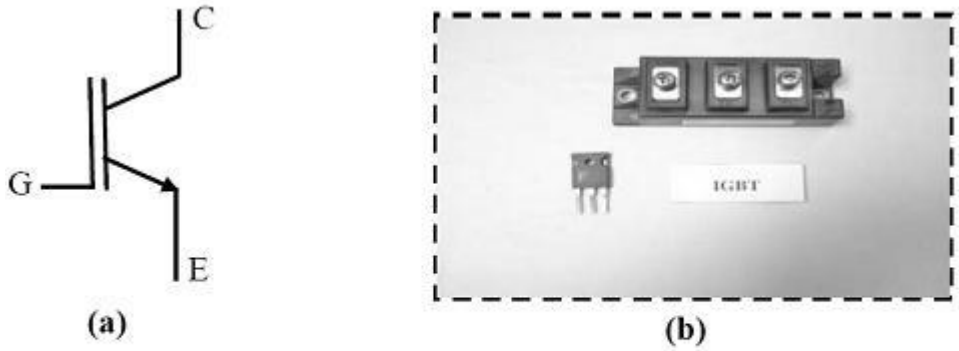


Fig. 15 Circuit symbol of an IGBT.
(a) Circuit symbol.
(b) Photograph.

Operating principle of an IGBT

Operating principle of an IGBT can be explained in terms of the schematic cell structure and equivalent circuit of Fig 16(a) and (c). From the input side the IGBT behaves essentially as a MOSFET. Therefore, when the gate emitter voltage is less than the threshold voltage no inversion layer is formed in the **p** type body region and the device is in the off state. The forward voltage applied between the collector and the emitter drops almost entirely across the junction J_2. Very small leakage current flows through the device under this condition. In terms of the equivalent current of Fig 16(c), when the gate emitter voltage is lower than the threshold voltage the driving MOSFET of the Darlington configuration remains off and hence the output **p-n-p** transistor also remains off.

When the gate emitter voltage exceeds the threshold, an inversion layer forms in the **p** type body region under the gate. This inversion layer (channel) shorts the emitter and the drain drift layer and an electron current flows from the emitter through this channel to the drain drift region. This in turn causes substantial hole injection from the **p+** type collector to the drain drift region. A portion of these holes recombine with the electrons arriving at the drain drift region through the channel. The rest of the holes cross the drift region to reach the p type body where they are collected by the source metallization.

From the above discussion it is clear that the n type drain drift region acts as the base of the output **p-n-p** transistor. The doping level and the thickness of this layer determines the current gain –a‖ of the **p-n-p** transistor. This is intentionally kept low so that most of the device current flows through the MOSFET and not the output **p-n-p** transistor collector. This

helps to reduced the voltage drop across the ‑body‖ spreading resistance shown in Fig 16 (b) and eliminate the possibility of static latch up of the IGBT.

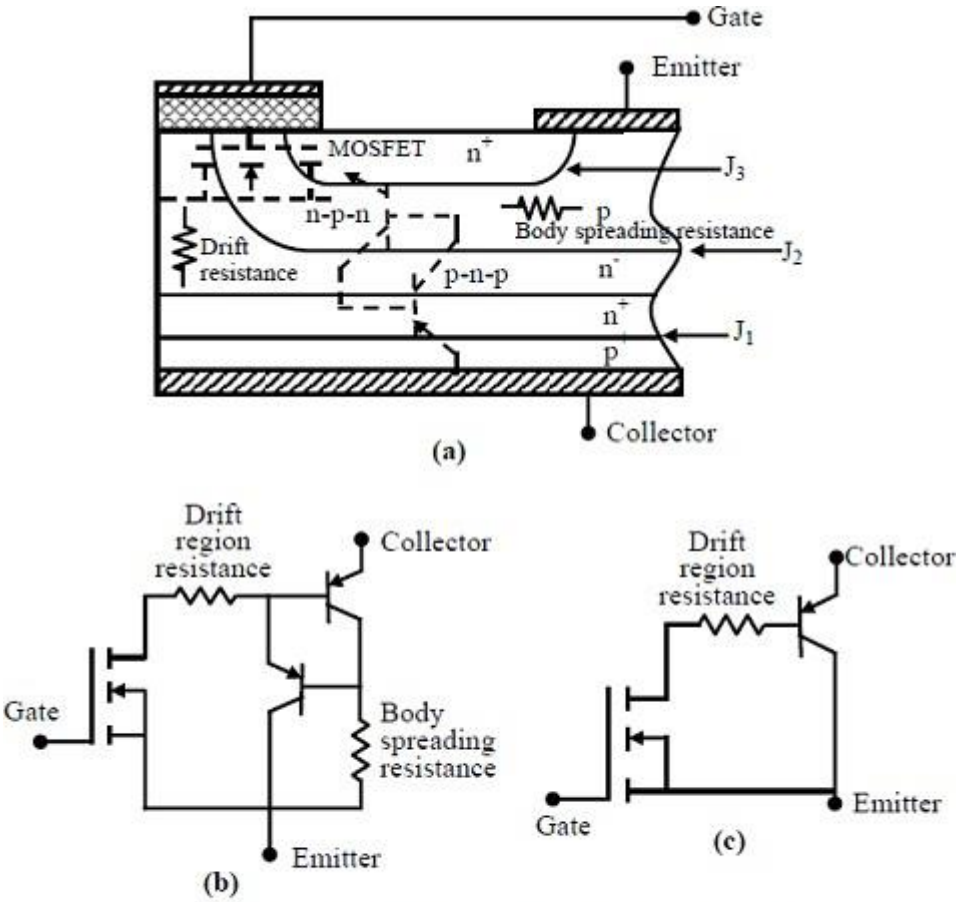


Fig.16 Parasitic thyristor in an IGBT cell.
(a) Schematic structure
(b) Exact equivalent circuit.
(c) Approximate equivalent circuit

The total on state voltage drop across a conducting IGBT has three components. The voltage drop across J_1 follows the usual exponential law of a **pn** junction. The next component of the voltage drop is due to the drain drift region resistance. This component in an IGBT is considerably lower compared to a MOSFET due to strong conductivity modulation by the injected minority carriers from the collector. This is the main reason for reduced voltage drop across an IGBT compared to an equivalent MOSFET. The last component of the voltage drop across an IGBT is due to the channel resistance and its magnitude is equal to that of a comparable MOSFET.

Steady state characteristics of an IGBT

The i-v characteristics of an n channel IGBT is shown in Fig 17 (a). They appear qualitatively similar to those of a logic level BJT except that the controlling parameter is not a base current but the gate-emitter voltage.

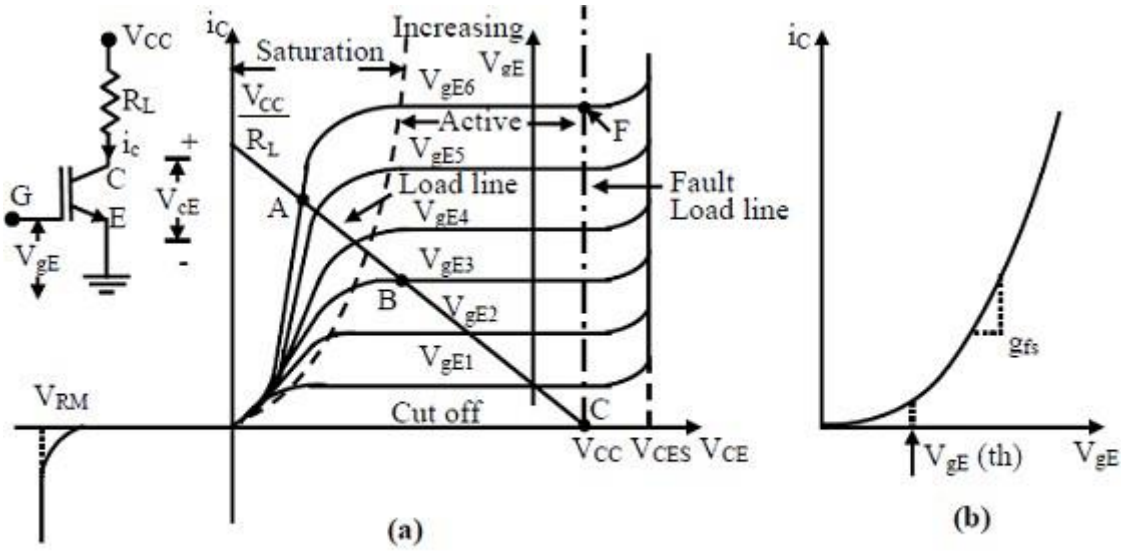


Fig. 17 Static characteristics of an IGBT
(a) Output characteristics; (b) Transfer characteristics

When the gate emitter voltage is below the threshold voltage only a very small leakage current flows though the device while the collector – emitter voltage almost equals the supply voltage (point C in Fig 17(a)). The device, under this condition is said to be operating in the cut off region. The maximum forward voltage the device can withstand in this mode (marked V_{CES} in Fig 17 (a)) is determined by the avalanche break down voltage of the body – drain **p-n** junction. Unlike a BJT, however, this break down voltage is independent of the collector current as shown in Fig 17(a). IGBTs of Non-punch through design can block a maximum reverse voltage (V_{RM}) equal to V_{CES} in the cut off mode. However, for Punch Through IGBTs V_{RM} is negligible due to the presence of the heavily doped **n+** drain buffer layer.

As the gate emitter voltage increases beyond the threshold voltage the IGBT enters into the active region of operation. In this mode, the collector current i_c is determined by the transfer characteristics of the device as shown in Fig 17(b). This characteristic is qualitatively similar to that of a power MOSFET and is reasonably linear over most of the collector current range. The ratio of i_c to ($V_{gE} - v_{gE(th)}$) is called the forward transconductance (g_{fs}) of the device and is an important parameter in the gate drive circuit design. The collector emitter voltage, on the other hand, is determined by the external load line ABC as shown in Fig 17(a).

As the gate emitter voltage is increased further i_c also increases and for a given load resistance (R_L) v_{CE} decreases. At one point v_{CE} becomes less than vgE – v_{gE}(th). Under this condition the driving MOSFET part of the IGBT (Fig 16(c)) enters into the ohmic region and drives the output **p-n-p** transistor to saturation. Under this condition the device is said to be in the saturation mode. In the saturation mode the voltage drop across the IGBT remains almost constant reducing only slightly with increasing v_{gE}.

In power electronic applications an IGBT is operated either in the cut off or in the saturation region of the output characteristics. Since v_{CE} decreases with increasing $v_{gE,}$ it is desirable to use the maximum permissible value of v_{gE} in the ON state of the device. v_{gE}(Max) is limited by the maximum collector current that should be permitted to flow in the IGBT as dictated by the ―latch-up‖ condition discussed earlier. Limiting V_{gE} also helps to limit the fault current through the device. If a short circuit fault occurs in the load resistance R_L (shown in the inset of Fig 17(a)) the fault load line is given by CF. Limiting v_{gE} to v_{gE6} restricts the fault current corresponding to the operating point F. Most IGBTs are designed to with stand this fault current for a few microseconds within which the device must be turned off to prevent destruction of the device.

1.8.2 Applications of IGBT:

IGBTs are used in high power applications such as:

- Appliance motor drives
- Electric vehicle motor drives
- Power factor correction converters
- Uninterruptible power supplies
- Solar inverters
- High frequency welders
- Inductive heating cookers

Chapter – 2 SCR CONTROL CIRCUITS

SCR or silicon controlled rectifier is a controlled device and it behaves as a short circuit while in the on state and as open circuit when in off condition.

2.1 Turn On Methods

2.1.1 Describe briefly different methods of TURN ON of an SCR

Turn-on method is otherwise known as triggering method. The turning on Process of the SCR is known as Triggering. In other words, turning the SCR from Forward-Blocking state to Forward-Conduction state is known as Triggering.

The various SCR triggering methods are

- Forward Voltage Triggering
- Thermal or Temperature Triggering
- Radiation or Light triggering
- dv/dt Triggering
- Gate Triggering

(a) Forward Voltage Triggering:-

In this mode, an additional forward voltage is applied between anode and cathode. When the anode terminal is positive with respect to cathode (V_{AK}) , Junction J_1 and J_3 is forward biased and junction J_2 is reverse biased. No current flows due to depletion region in J_2 is reverse biased (except leakage current). As V_{AK} is further increased, at a voltage V_{BO} (Forward Break Over Voltage) the junction J_2 undergoes avalanche breakdown and so a current flows and the device tends to turn ON (even when gate is open)

(b) Thermal (or) Temperature Triggering:-

The width of depletion layer of SCR decreases with increase injunction temperature. Therefore in SCR when V_{AR} is very near its breakdown voltage, the device is triggered by increasing the junction temperature. By increasing the junction temperature the reverse biased junction collapses thus the device starts to conduct.

(c) Radiation Triggering (or) Light Triggering:-

For light triggered SCRs a special terminal niche is made inside the inner P layer instead of gate terminal. When light is allowed to strike this terminal, free charge carriers are generated. When intensity of light becomes more than a normal value, the thyristor starts conducting. This type of SCRs are called as LASCR

(d) dv/dt Triggering:-

When the device is forward biased, J_1 and J_3 are forward biased, $J_2$is reverse biased. Junction J_2 behaves as a capacitor, due to the charges existing across the junction. If voltage across the device is V, the charge by Q and capacitance by C then,

$i_c=dQ/dt$

$Q=CV$

$i_c=d(CV)/dt =C.dV/dt+V.dC/dt$

As $dC/dt = 0$, $i_c = C.dV/dt$

Therefore when the rate of change of voltage across the device becomes large, the device may turn ON, even if the voltage across the device is small.

(e) Gate Triggering:-

This is most widely used SCR triggering method. Applying a positive voltage between gate and cathode can Turn ON a forward biased thyristor. When a positive voltage is applied at the gate terminal, charge carriers are injected in the inner P-layer, thereby reducing the depletion layer thickness. As the applied voltage increases, the carrier injection increases, therefore the voltage at which forward break-over occurs decreases.

2.1.2 General functions to be fulfilled by gate control circuits

The gate control circuit is also called the firing circuit and a firing circuit should fulfill the following two functions.

(i) If power circuit has more than one SCR, the firing circuit should produce gating pulses for each SCR at the desired instant for proper operation of the power circuit.

These pulses must be periodic in nature and the sequence of firing must correspond with the type of thyristorised power controller.

(ii) Before giving the voltage pulses to the firing circuit, the voltage pulses should be fed to a driver circuit. The reason is that the control signal generated by a firing circuit may not be able to turn-on the SCR.

2.2 Firing Circuits

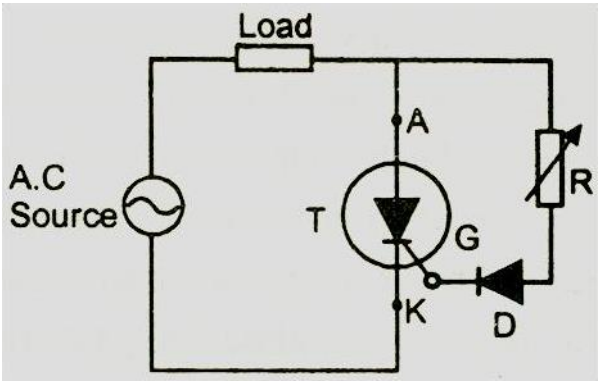
2.2.1 General layout diagram of firing circuit

The different firing circuits used are

- R-firing circuit
- RC-firing circuit
- UJT pulse trigger circuit
- Synchronous triggering (Ramp Triggering) circuit

2.2.2R firing circuits or Resistance triggering circuit:

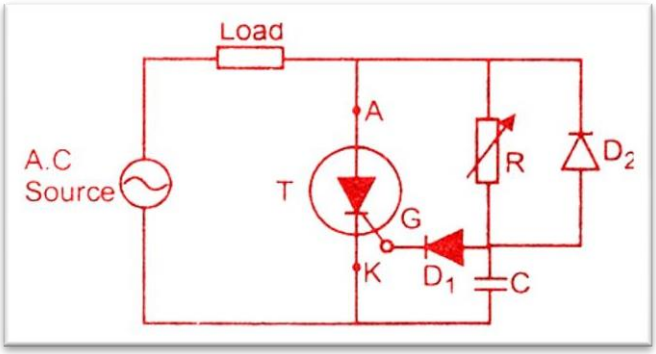
The following circuit shows the resistance triggering. In this method, the variable resistance R is used to control the gate current.



Depending upon the value of R, when the magnitude of the gate current reaches the sufficient value(latching current of the device) the SCR starts to conduct. The diode D is called as blocking diode. It prevents the gate cathode junction from getting damaged in the negative half cycle. By considering that the gate circuit is purely resistive, the gate current is in phase with the applied voltage. By using this method we can achieve maximum firing angle up to 90°.

2.2.3RC-firing circuit

The following circuit shows the resistance-capacitance triggering.



By using this method we can achieve firing angle more than 90°. In the positive half cycle, the capacitor is charged through the variable resistance R up to the peak value of the applied voltage. The variable resistor R controls the charging time of the capacitor. Depends upon the voltage across the capacitor, when sufficient amount of gate current will flow in the circuit, the SCR starts to conduct. In the negative half cycle, the capacitor C is charged up to the negative peak value through the diode D2. Diode D1 is used to prevent the reverse break down of the gate cathode junction in the negative half cycle.

2.2.4UJT pulse trigger circuit

One common application of the Uni-junction transistor is the triggering of the other devices such as the SCR, triac etc. The basic elements of such a triggering circuit are shown in figure. The resistor R_E is chosen so that the load line determined by R_E passes through the device characteristic in the negative resistance region, that is, to the right of the peak point but to the left of the valley point, as shown in figure. If the load line does not pass to the right of the peak point P, the device cannot turn on.

For ensuring turn-on of UJT $R_E < V_{BB} – Vp / I_P$

This can be established as below

Consider the peak point at which $I_{RE} = Ip$ and $V_E = V_P$

(the equality $I_{RE} = I_P$ is valid because the charging current of capacitor, at this instant is zero, that is, the capacitor, at this particular instant, is changing from a charging state to a discharging state).

Then $V_E = V_{BB} – I_{RE} R_E$

So, $R_{E(MAX)} = V_{BB} – V_E / I_{RE} = V_{BB} – Vp / I_P$ at the peak point.

At the valley point, V

$I_E = I_V$ and $V_E = V_V$ so that

$V_E = V_{BB} – I_{RE} R_E$

So $R_E(MIN) = V_{BB} – V_E / I_{RE} = V_{BB} – V_V / I_V$ or for ensuring turn-off.

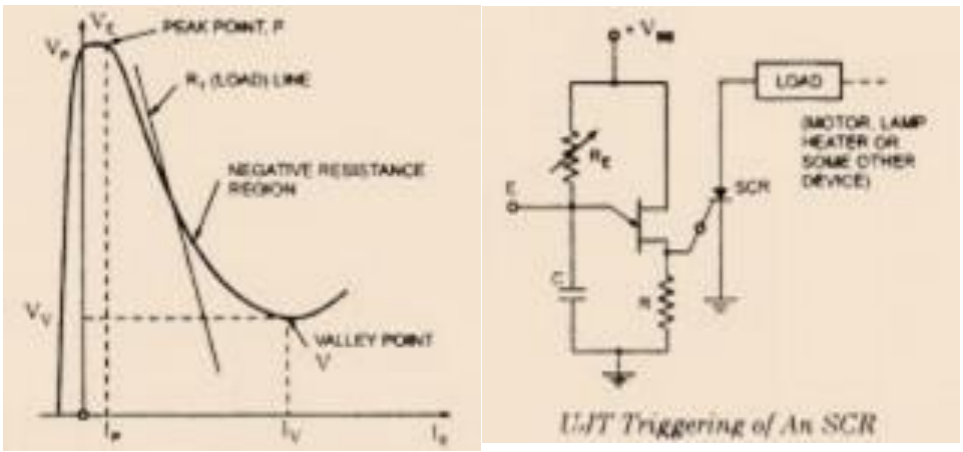
$R_E > = V_{BB} – V_V / I_V$

So, the range of resistor R_E is given as

$V_{BB} – V_P / I_P > R_E > V_{BB} – V_V / I_V$

The resistor R is chosen small enough so as to ensure that SCR is not turned on by voltage V_R when emitter terminal E is open or $I_E = 0$

The voltage $V_R = RV_{BB}/R + R_{BB}$ for open-emitter terminal.

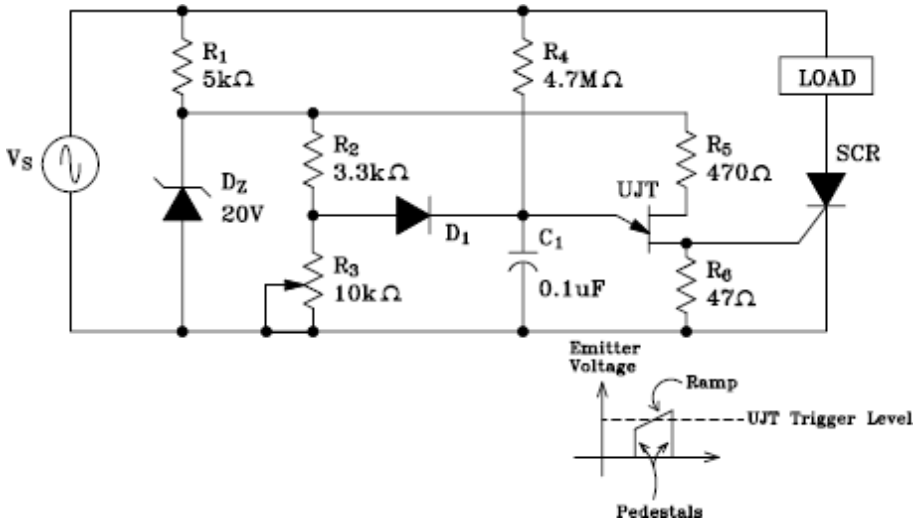


UJT Triggering of An SCR

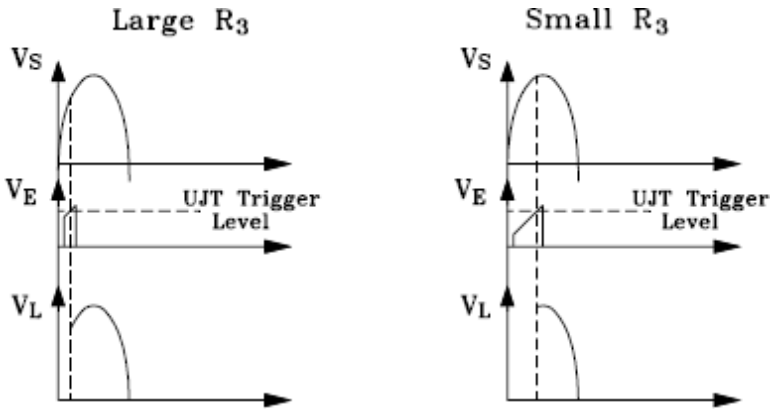
The capacitor C determines the time interval between triggering pulses and the time duration of each pulse. By varying R_E, we can change the time constant R_E C and alter the point at which the UJT fires. This allows us to control the conduction angle of the SCR, which means the control of load current.

2.2.5 Ramp-Pedestal UJT-SCR Control Circuit:

The circuit, shown below, uses a UJT to trigger a SCR. The UJT is used to more accurately trigger the SCR. When the source voltage exceeds 20V, the zener diode (D_Z) will begin to conduct, applying a DC voltage across the base connections of the UJT. At the same time, diode D_1 will be forward biased, and the capacitor will quickly charge through R_1 and R_2. This represents the left-hand pedestal portion of the of the emitter voltage.



Once the capacitor charges to the voltage across R_3, D_1 will become reverse biased and the capacitor will continue to slowly charge through R_4. This represents the ramp portion of the emitter voltage.



The capacitor continues to charge until the UJT fires. At this point the capacitor will quickly discharge through R_6, and this represents the right-hand pedestal of the emitter voltage. The capacitor discharge is sufficient to trigger the SCR. The point at which the UJT fires can be adjusted by varying the pot R3. With a large setting on R3, the capacitor must charge to a larger value before D2 becomes reverse biased. This causes the UJT to fire faster, resulting in more of the source voltage appearing across the SCR. This can be seen graphically as shown in the fig.

2.3 Turn-off methods (Communication Schemes)

The term commutation basically means the transfer of current from one path to another. It is not possible for a thyristor to turn itself OFF; the circuit in which it is connected must reduce the thyristor current to zero to enable it to turn-off.

2.3.1 Definition

'COMMUTATION' is the term to describe the methods of achieving this, or it is defined as the process of turning-off a thyristor.

2.3.2 List different types of communication methods

Broadly classified into two methods:

1. Natural commutation
2. Forced commutation

Natural commutation

This widely used method of commutation makes use of the alternating, reversing nature of a.c voltage to effect the current transfer. As the current passes through natural zero, a reverse voltage will simultaneously appear across the device. This immediately turns-off the device. This process is called as natural commutation since no external circuit is required for this purpose.

Forced commutation

In case of d.c circuits, for switching off the thyristors, the forward current should be forced to be zero by means of some external circuits. The process is called forced commutation.

Classification of forced commutation techniques

The classification is based on the arrangement of commutating components and the manner in which zero current is obtained in the SCR. The six distinct classes by which the SCR can be turned off are:

Class A Self commutated by a resonating load

Class B Self commutated by a L-C circuit

Class C C or L-C switched by another load carrying SCR otherwise known as Complementary commutation

Class D C or L-C switched by an auxiliary SCR, known as Auxiliary commutation

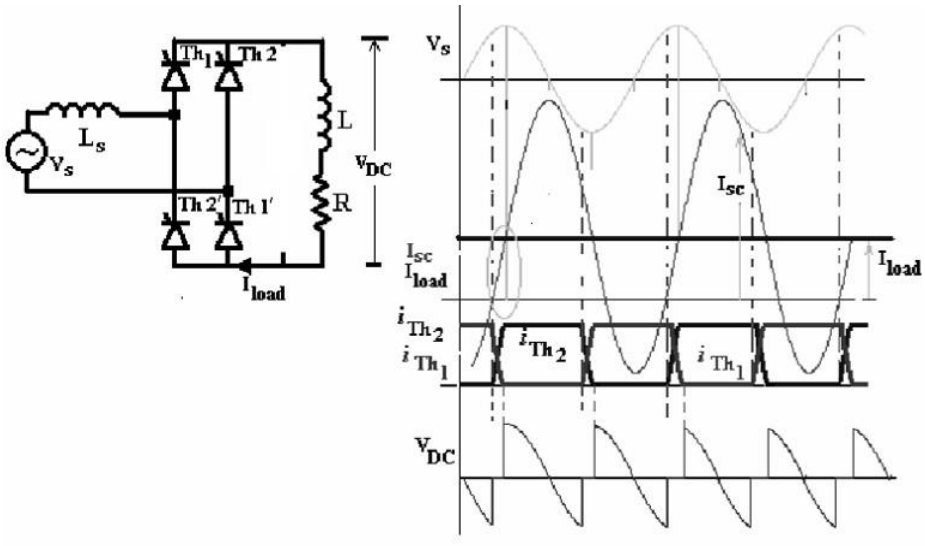
Class E An external pulse source for commutation, also known as External pulse commutation

Class F or AC line commutation or natural commutation

2.3.3 Different commutation with circuit diagram and waveforms

a) Line commutation or Class-F commutation

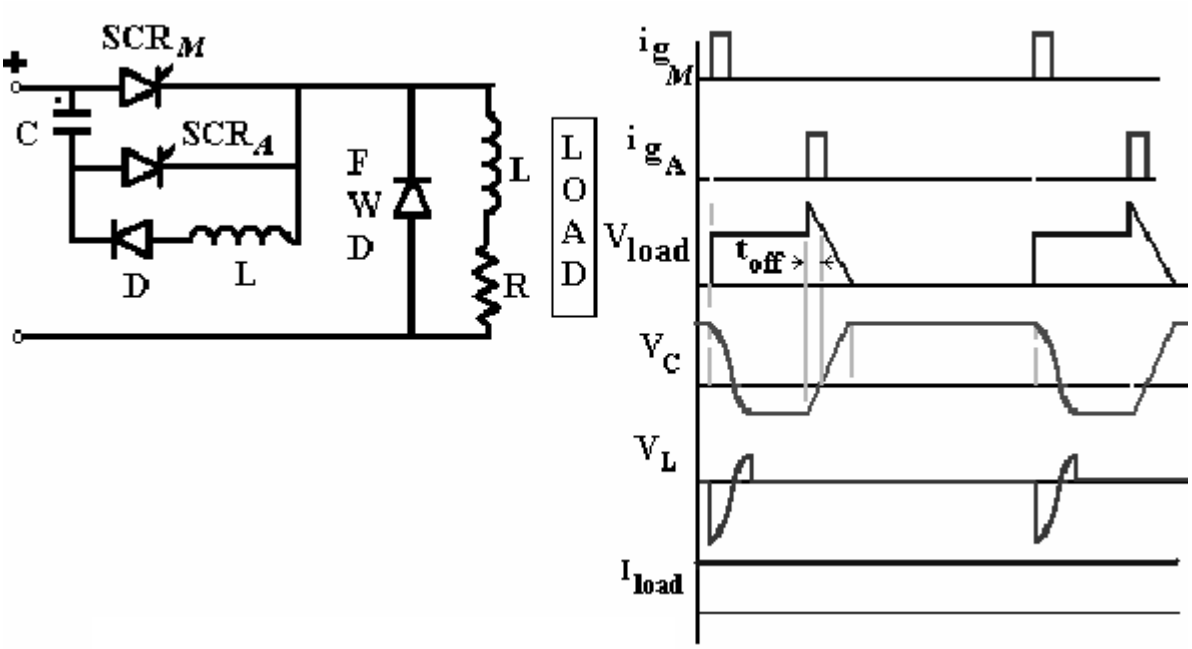
If the supply is an alternating voltage, load current will flow during the positive half cycle. With a highly inductive load, the current may remain continuous for some time till the energy trapped in the load inductance is dissipated. During the negative half cycle, therefore, the SCR will turn off when the load current becomes zero 'naturally'. The negative polarity of the voltage appearing across the outgoing SCR turns it off if the voltage persists for the rated turnoff period of the device. The duration of the half cycle must be definitely longer than the turnoff time of the SCR. The rectifier in the below figure is supplied from a single phase AC supply. The commutation process involved here is representative of that in a three phase converter. The converter has an input inductance L_s arising mainly out of the leakage reactance of the supply transformer. Initially, SCRs $Th_1$and $Th_{1'}$ are considered to be conducting. The triggering angle for the converter is around 60^0. The converter is operating in the continuous conduction mode aided by the highly-inductive load. When the incoming SCRs, Th2and Th2' are triggered, the current through the incoming devices cannot rise instantaneously to the load current level. A circulating current Isc builds up in the short-circuited path including the supply voltage, Vs-Ls-$Th_{1'}$- Th_2 and Vs- Ls-$Th_{2'}$-Th_1 paths. The period when both the devices conduct is known as the 'overlap period'. Since all SCRs are in conduction, the output voltage for this period is zero. If the 'fully-controlled' converter in the figure is used as an inverter with triggering angles > 90^0, the converter triggering can be delayed till the 'margin angle' which includes the overlap angle and the turn-off time of the SCR - both dependent on the supply voltages.



Class F, natural commutation by supply voltage

b) Auxiliary voltage commutation or Class-D commutation

The following circuit is used for auxiliary voltage commutation. SCR_A must be triggered first in order to charge the upper terminal of the capacitor as positive. As soon as C is charged to the supply voltage, SCR_A will turn off.

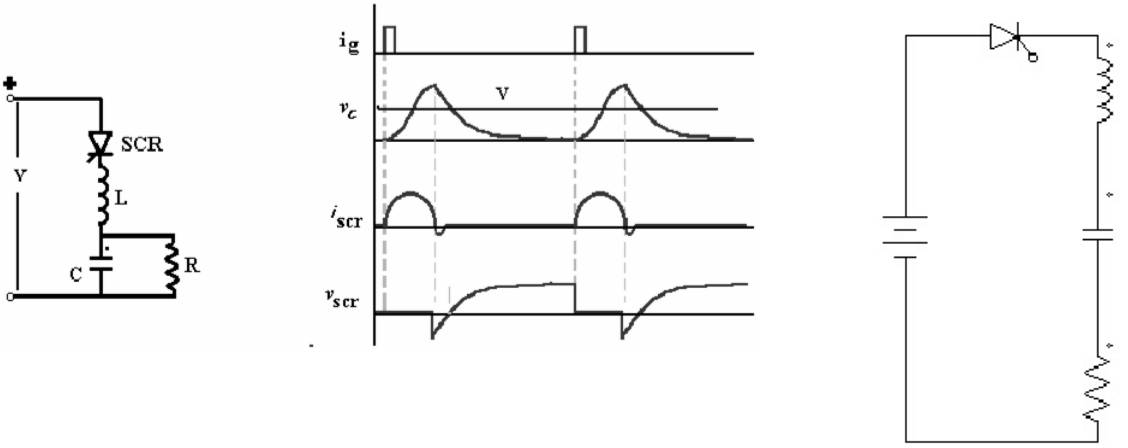


When SCR_M is triggered the current flows in two paths:

- Load current flows through the load and
- The commutating current flows through C- SCR_M -L-D network.

The charge on C is reversed and held at that level by the diode D. When SCR_A is re-triggered, the voltage across C appears across SCR_M via SCR_A and SCR_M is turned off. If the load carries a constant current as in Fig. the capacitor again charges linearly to the dot as positive.

c) Resonant commutation or Class-A commutation



When the SCR is triggered, anode current flows and charges up C with the dot as positive. The L-C-R forms a second order under-damped circuit. The current through the SCR builds up and completes a half cycle. When the inductor current will then attempt to flow through the SCR in the reverse direction and the SCR will be turned off. Load can be either in parallel with capacitance or in series with the capacitance as in fig below. The capacitor voltage is at its peak when the SCR turns off and the capacitor discharges into the resistance in an exponential manner .The SCR is reverse-biased till the capacitor voltages returns to the level of the supply voltage V.

Chapter-3 CONTROLLED RECTIFIER

Introduction

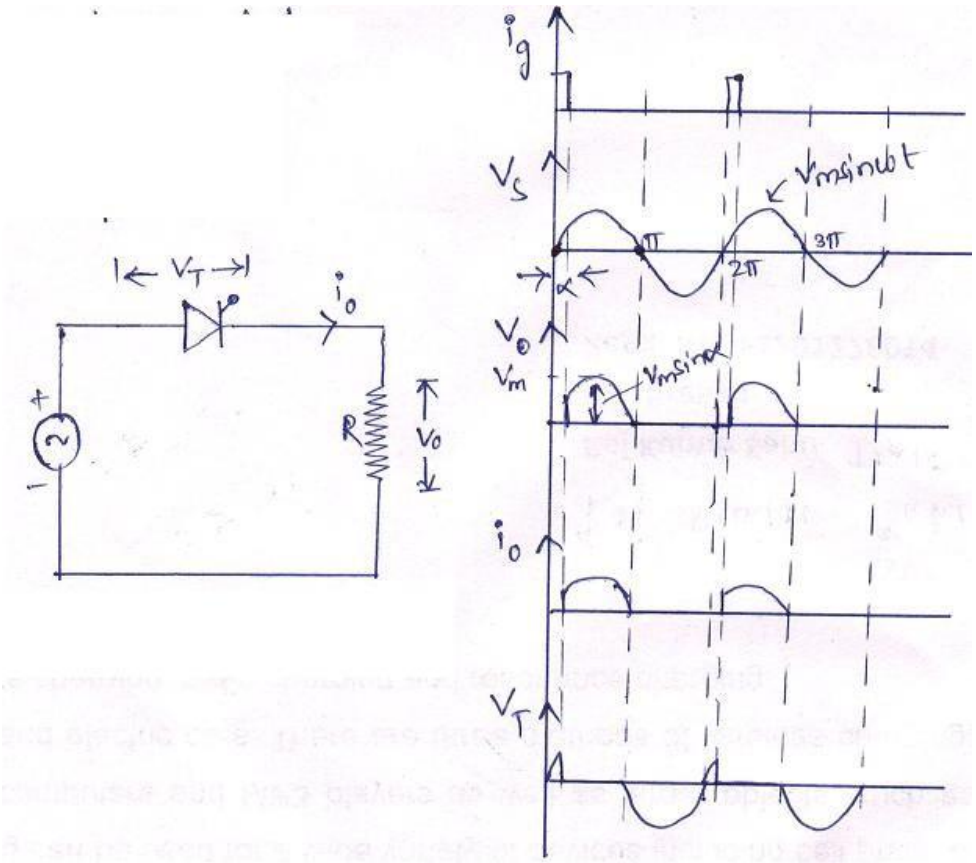
Single phase fully controlled bridge converters are widely used in many industrial applications. They can supply unidirectional current with both positive and negative voltage polarity. Thus they can operate either as a controlled rectifier or an inverter. The inverter mode of operation of a single phase fully controlled converter is made possible by the forward voltage blocking capability of the thyristors which allows the output voltage to go negative. The disadvantages of the single phase fully controlled converter are also related to the same capability.

Application

Used in high voltage DC transmission, electrometallurgical process, magnetic power supplies, electroplating, battery charging, speed control of Dc drives, Traction.

3.1 Controlled rectifiers Techniques (Phase Angle, Extinction Angle control & PWM) and 3.3 principle of phase control and definition of firing angle (alpha) and Conduction angle (beta) with schematic diagram and waveforms for half wave controlled rectifier

Principle of phase control



A simple controlled rectifier circuit consists of a single thyristor feeding dc power to a resistive load R. source voltage is $v_s = v_m \sin wt$.

An SCR can conduct only when anode voltage is positive and a gating signal is applied. A thyristor blocks the flow of load current i_o until it is triggered.

At some delay angle α, a positive gate signal is applied between gate and cathode turns on the SCR. Immediately full supply voltage is applied to the load as v_o.

Firing Angle(α): - It is the angle between the instant at which the thyristor would conduct, if it was a diode, and the instant at which it is triggered.

It can also be defined as the angle measured from the instant SCR gets forward biased to the instant it is triggered.

Conduction Angle(γ): - it is defined as the angle during the period in which the SCR is in conduction state.

Extinction Angle(β): - it is the angle measured from the reference point to the instant at which the current extinguishes to zero.

Relation between β, γ and α

$\beta = \alpha + \gamma$

3.2 Classification of converters: -

The phase controlled converters may be classified as semi-converter, full converter, dual converter. Depending on the input ac supply used they are classified as single phase and three phase converters.

Semi-converter: -A semi-converter is a one quadrant converter and it has one polarity of output voltage and current. It contains a mixture of diodes and thyristors allowing more limited control over the dc output voltage level than the full controlled rectifier. It is cheaper. It permits power flow from AC system to DC load. It is also known as half-wave controlled converter.

Full-converter: -A full-converter is a two-quadrant converter and the polarity of its output voltage can be either positive or negative. However, the output current of full-converter has one polarity only. Here power can be transmitted from AC side to DC side (conversion) and from DC side to AC side (inversion). It uses only thyristor as rectifying elements.

Dual-converter: -If two full converters are connected back to back they form a dual converter. It can operate in four quadrants and both the output voltage and current can be either positive or negative. Normally these are used in high power applications.

3.4 Integral Cycle Control (ICC)

For power transfer two types of controls are normally used. One is on-off control or integral cycle control and another is phase angle control.

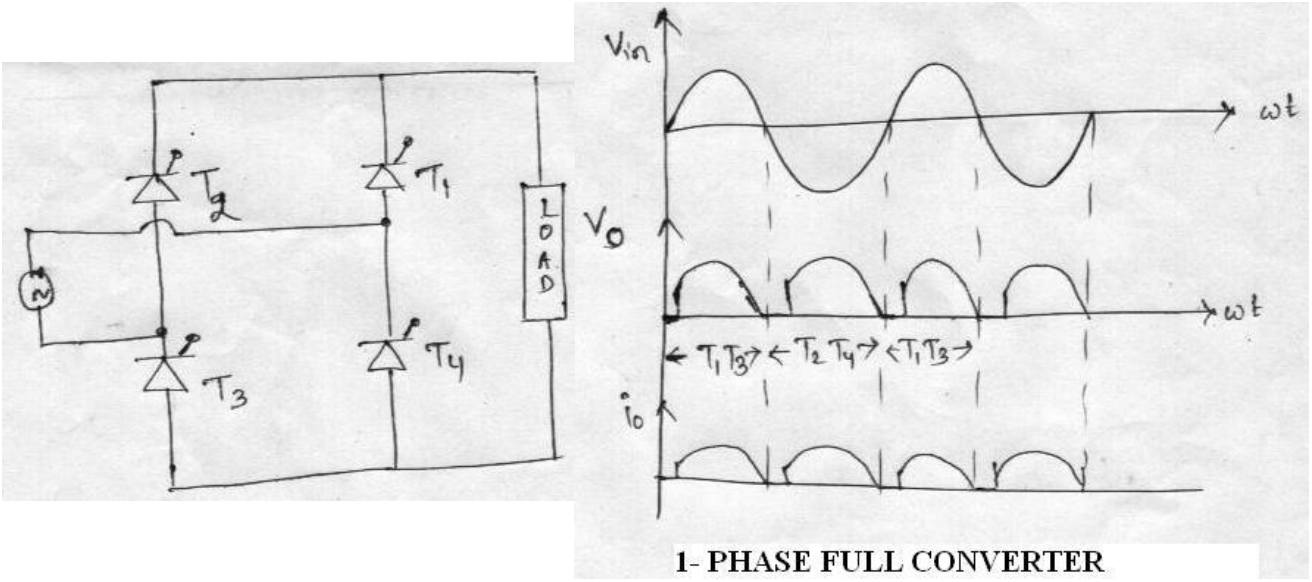
In integral-cycle control, thyristor switches connect the load to the ac source for a few cycles of input voltage and disconnects it for another few cycles.

The ICC is otherwise known as burst firing or zero voltage switching or cycle selection.

3.6 Single phase fully controlled bridge converter with Resistive load only (with & without FD)

The figure shows the circuit diagram of a single phase fully controlled bridge converter. It is one of the most popular converter circuits and is widely used in the speed control of separately excited dc machines.

The single phase fully controlled bridge converter is obtained by replacing all the diode of the corresponding uncontrolled converter by thyristors. Thyristors T1 and T2 are fired together while T3 and T4 are fired 180º after T1 and T2. From the circuit diagram of Fig 10.3(a) it is clear that for any load current to flow at least one thyristor from the top group (T1, T3) and one thyristor from the bottom group (T2, T4) must conduct and neither T1T3 nor T2T4 can conduct simultaneously. Whenever T3 and T4 are in the forward blocking state and a gate pulse is applied to them, they turn ON and at the same time a negative voltage is applied across T1 and T2 commutating them immediately. Similar is the case for T1 and T2.



1- PHASE FULL CONVERTER

The only possible conduction modes when the current i_0 can flow are T1T2 and T3T4. It may happen that at a given moment none of the thyristors conduct. This situation will typically occur when the load current becomes zero in between the firings of T1T2 and T3T4. Once the load current becomes zero all thyristors remain off.

In this mode the load current remains zero. Consequently the converter is said to be operating in the discontinuous conduction mode. Figure shows the voltage across different devices and the dc output voltage during each of these conduction modes. It is to be noted that whenever T1 and T2 conducts, the voltage across T3 and T4 becomes $-v_i$. Therefore T3 and T4 can be fired only when v_i is negative i.e, over the negative half cycle of the input supply voltage. Similarly T1 and T2 can be fired only over the positive half cycle of the input supply. The voltage across the devices when none of the thyristors conduct depends on the off state impedance of each device.

Under normal operating condition of the converter the load current may or may not remain zero over some interval of the input voltage cycle. If i_0 is always greater than zero then the converter is said to be operating in the continuous conduction mode. In this mode of operation of the converter T1T2 and T3T4 conducts for alternate half cycle of the input supply.

3.7 Explain with circuit diagram and waveforms the operation of fully controlled three phase bridge converter with Restive load (with & with out FD)

3Φ full Converter using Bridge Circuit

3Φ phase power supply are connected in two ways.

(1) Star connection

(2) Delta connection

In a 3Φ full converter bridge rectifier circuit two thyristor phases are required each phase with 6 SCR in a circuit. This configuration utilizes both the positive and negative portion of input signal.

The thyristors are fired at an interval of $\pi/3$ at wt= $(\pi/6)+\alpha$.

The thyristor are fired at an interval of $\pi/3$ at wt = $\pi/6+\alpha$, thyristor T6 is already conducting & thyristor T1 is turned on. During the interval $(\pi/6+\alpha) \leq wt \leq (\pi/2+\alpha)$ thyristor T1 & T6 are conduct the line to line voltage $V_{ab}= V_{an} -V_{bn}$ appears across the load. At wt = $(\pi/2)+\alpha$ thyristor T2 is fired & thyristor T6 reverse biased immediately T6 is turned off due to natural commutation. During the interval $(\pi/2+\alpha) \leq wt \leq (5\pi/6+\alpha)$ thyristor T1 & T2 conduct & the line to line voltage V_{ac} appears across the load. The firing sequence is 12,23,34,45,56,61

LINE TO NEUTRAL VOLTAGE

Let

$V_{an} = V_m \sin wt$

$V_{bn} = V_m \sin (wt-2\pi/3)$

$V_{cn} = V_m \sin (wt+2\pi/3)$

Line to line voltage is

$V_{ab} = V_{an} - V_{bn} = \sqrt{3}\ V_m \sin (wt+\pi/6)$

$V_{bc} = V_{bn} - V_{cn} = \sqrt{3}\ V_m \sin(wt-\pi/2)$

$V_{ca} = V_{cn} - V_{an} = \sqrt{3}\ V_m \sin(wt+\pi/2)$

The average o/p voltage

$$V_{dc} = 3/\pi \int_{\frac{\pi}{6}+\alpha}^{\frac{\pi}{2}+\alpha} Vab$$

$$= 3/\pi \int_{\frac{\pi}{6}+\alpha}^{\frac{\pi}{2}+\alpha} \sqrt{3}Vm \sin\left(wt + \frac{\pi}{6}\right) d\,(wt)$$

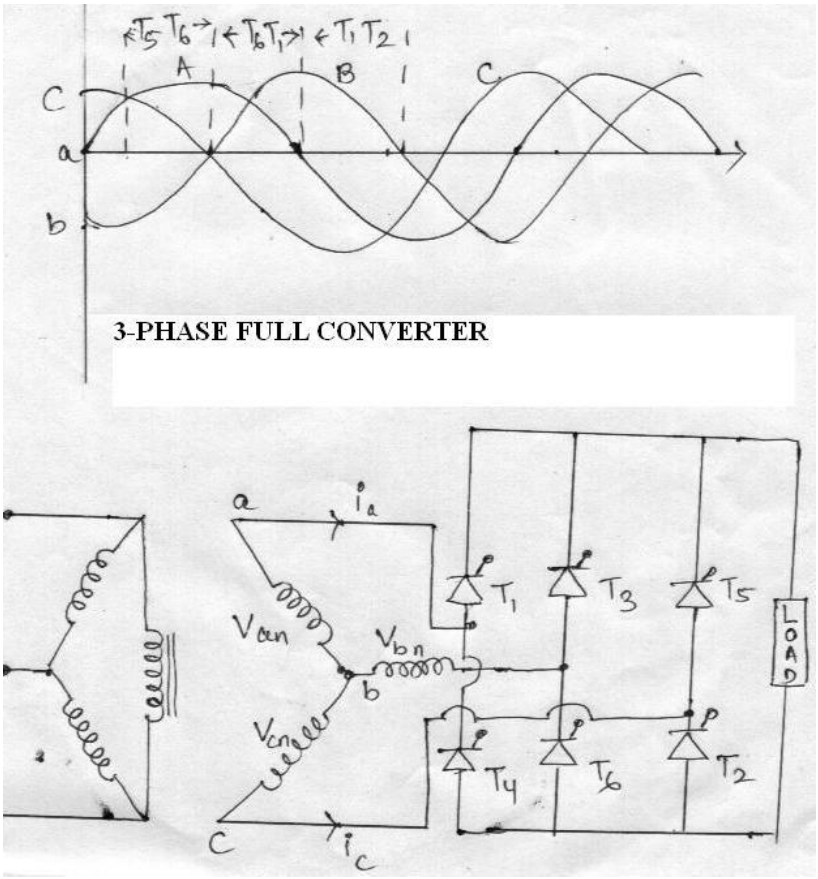
$= 3\sqrt{3}\ V_m \cos \alpha / \pi$ For $\alpha=0$

$$V_{dm} = 3\sqrt{3}V_m/\pi$$

GATING SEQUENCE:-

Generate a pulse signal at the +ve zero crossing of the phase voltage Vam delay the pulse the desired angle $\alpha+\pi/6$ & apply it to the gate & cathode terminal of T1 through a gate isolating ckt.

Generate 5 more pulses each delayed by $\pi/6$ from each other for getting T1,T2,T3,T4,T5 & T6 respectively through gate isolating ckt.



Chapter-4 CHOPPER

4.1 Define chopper & its applications.

The fixed voltage of a dc source can be converted to a variable average voltage on a load by placing a high speed switch between the dc source and the load. This high speed static switch is called chopper. This high speed switch used may be a thyristor or a BJT or an IGBT or a power MOSFET or may be a GTO depending on the application.

Thus a chopper is a power electronic device that converts a power directly from fixed dc to variable dc. In other words a chopper is a dc to dc converter.

There are three basic types of dc-dc converter circuits, termed as buck, boost and buck-boost. In all of these circuits, a power device is used as a switch. The buck converter (dc-dc) is called as _step-down chopper‘, whereas boost converter (dc-dc) is a _step-upchopper‘.

Applications of chopper

Choppers find their applications in traction motors, trolley cars, hoists and also in variable speed ac and dc drives.

The advantages of chopper include smooth speed control, low losses, high efficiency, fast dynamic response and regeneration capability when applied in drive control.

4.2 Principle of operation of

- **Step down chopper (Buck converts)**

A buck converter (dc-dc) is shown in the below figure. Only a switch is shown in this figure. Also a diode (termed as freewheeling) is used to allow the load current to flow through it, when the switch (i.e., a device) is turned off.

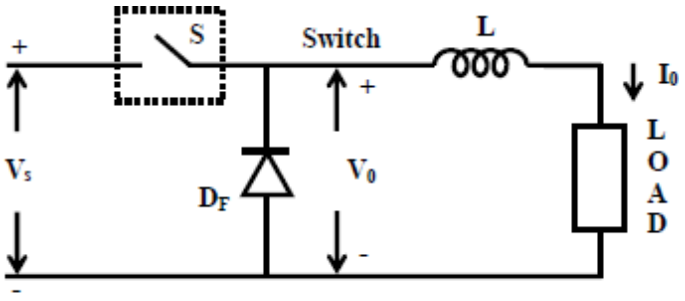


Fig. 17.1(a): Buck converter (dc-dc)

The load is inductive (R-L) one. Due to the load inductance, the load current must be allowed a path, which is provided by the diode; otherwise, i.e., in the absence of the above

diode, the high induced emf of the inductance, as the load current tends to decrease, may cause damage to the switching device. If the switching device used is a thyristor, this circuit is called as a step-down chopper, as the output voltage is normally lower than the input voltage. The output voltage and current waveforms of the circuit are shown below.

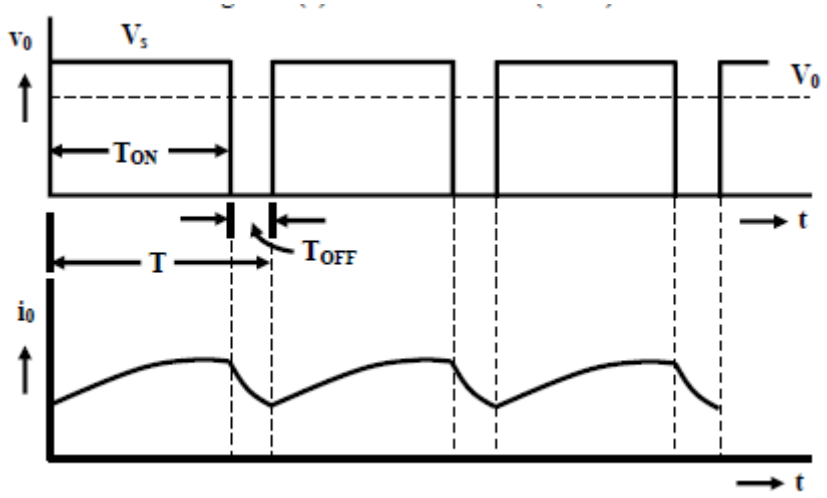


Fig. 17.1(b): Output voltage and current waveforms

The output voltage is same as the input voltage, i.e., $V_s = V_0$, when the switch is ON, during the period, $T_{ON} \geq t \geq 0$. The switch is turned on at t = 0, and then turned off at t= T_{ON}. This is called ON period.

During the next time interval, $T \geq t \geq T_{ON}$, the output voltage is zero, i.e., $V_0 = 0$, as the diode D_F, now conducts.

The OFF period is $T_{OFF} = T - T_{ON}$ with the time period being

$T = T_{ON} + T_{OFF}$.

The frequency is $f = 1/T$.

The duty ratio is $k = T_{ON}/T = (T_{ON})/(T_{ON} + T_{OFF})$],

its range being $1.0 \geq k \geq 0.0$

- ## Step down chopper (Boost converts)

A boost converter (dc-dc) is shown in below figure. A diode is used in series with the load. An inductance, L is assumed in series with the input supply. First the switch, S (i.e., the device) is put ON (or turned ON) during the period, $T_{ON} \geq t \geq 0$ the ON period being T_{ON} The output voltage is zero if no battery (back emf) is connected in series with the load, The current from the source (i_s) flows in the inductance L. The value of current increases linearly with time in this interval, with (di/ dt) being positive.

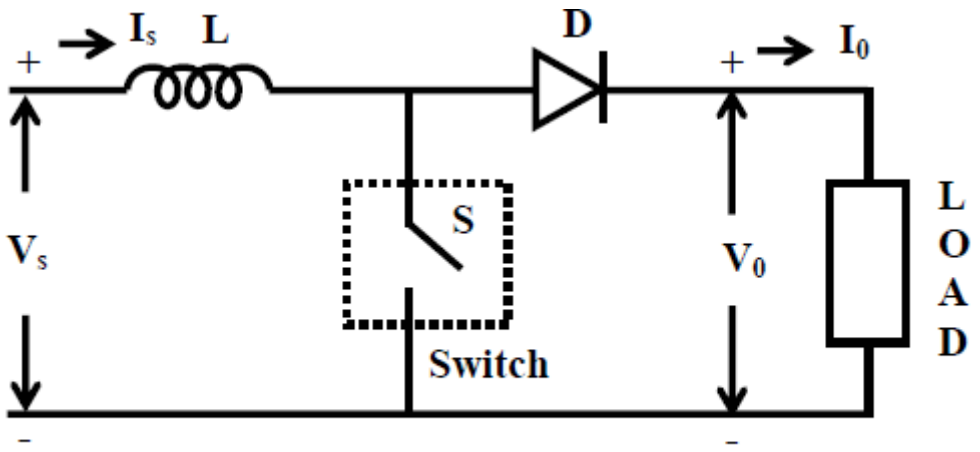


Fig. 17.2(a): Boost converter (dc-dc)

As the current through L increases, the polarity of the induced emf is taken as say, positive, the left hand side of L being +ve. The equation for the circuit is,

$$V_s = L\frac{di_s}{dt} \qquad \text{or,} \quad \frac{di_s}{dt} = \frac{V_s}{L}$$

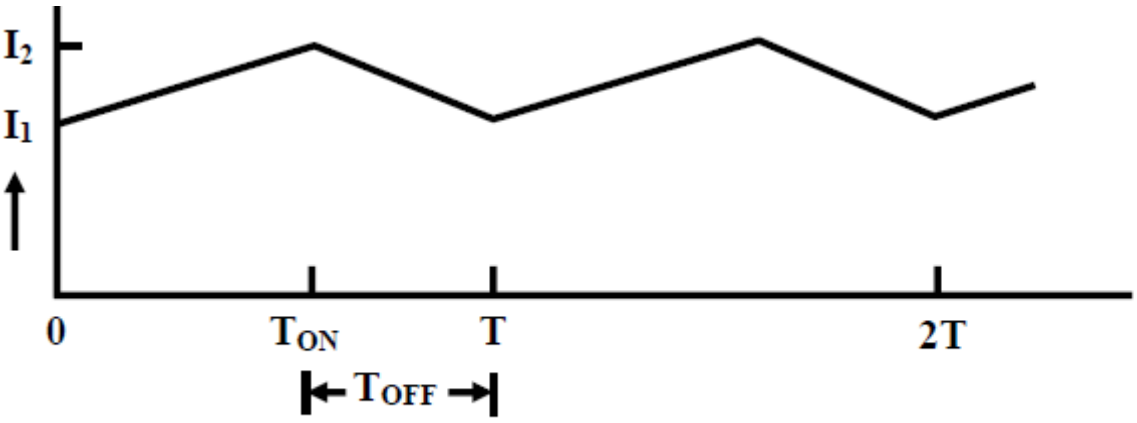


Fig. 17.2(b): Waveforms of source current (i_S)

The switch, S is put OFF during the period, $T \geq t \geq T_{ON.}$

As the current through L decreases, with its direction being in the same direction as shown (same as in the earlier case), the induced emf reverses, the left hand side of L being -ve. So, the induced emf (taken as –ve in the equation given later) is added with the supply voltage, being of the same polarity, thus, keeping the current $i_s = i_0$ in the same direction. The current $i_s = i_0$ decreases linearly in the time interval, T_{OFF} as the output voltage is assumed to be nearly constant. In this case, the output voltage is higher than the input voltage, as

contrasted with the previous case of buck converter (dc-dc). So, this is called boost converter (dc-dc), when a self-commutated device is used as a switch.

- **Step up & Down chopper (Buck Boost converts)**

The below figure shows a buck-boost converter. The connection of the diode may be noted, as compared with its connection in a boost Converter. The inductor, L is connected in parallel after the switch and before the diode. The load is of the same type as given earlier. A capacitor, C is connected in parallel with the load. The polarity of the output voltage is opposite to that of input voltage here. When the switch, S is put ON, the supply current(is) flows through the path, V_S-S-L during the time interval, T_{ON} The currents through both source and inductor increase and are same, with di_L/dt being positive.

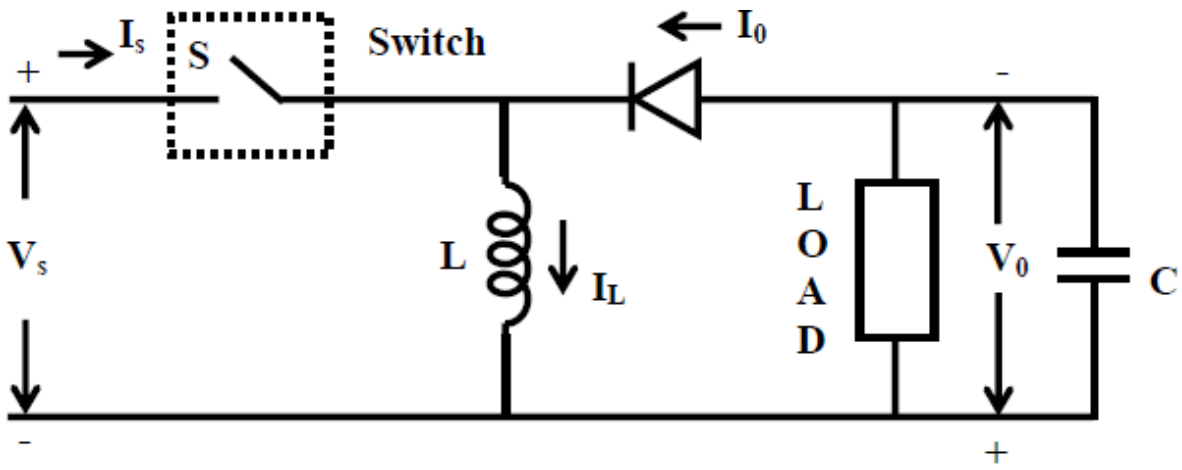


Fig. 17.3(a): Buck-boost converter (dc-dc)

The polarity of the induced voltage is same as that of the input voltage. The equation for the circuit is,

$$V_s = L\frac{di_L}{dt} \qquad \text{or,} \quad \frac{di_L}{dt} = \frac{V_s}{L}$$

Then, the switch, S is put OFF. The inductor current tends to decrease, with the polarity of the induced emf reversing. di_L/dt is negative now, the polarity of the output voltage,V_0 being opposite to that of the input voltage, V_S.

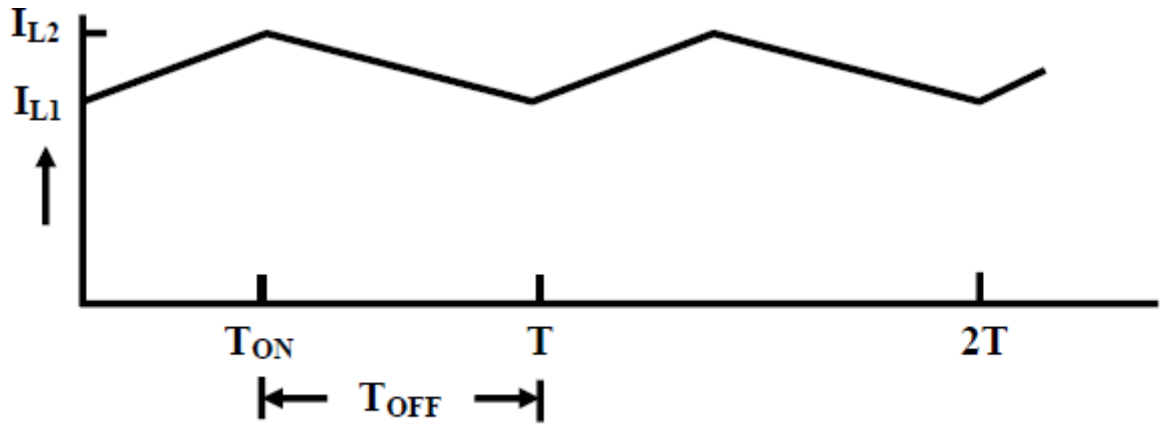


Fig. 17.3(b): Inductor current (i_L) waveform

The path of the current is through L, parallel combination of load & C, and diode D, during the time interval, T_{OFF}. The output voltage remains nearly constant, as the capacitor is connected across the load.

4.3 Control Strategies of chopper (TRC & Current unit)

In all cases, it is shown that the average value of the output voltage can be varied. The two types of control strategies (schemes) are employed in all cases. These are:

(a) Time-ratio control, and (b) Current limit control

Time-ratio control (TRC)

In the time ratio control the value of the duty ratio, $k=T_{ON}/T$ is varied. There are two ways, which are constant frequency operation, and variable frequency operation.

Constant Frequency Operation

In this control strategy, the ON time, T_{ON} is varied, keeping the frequency or time period f = 1/T constant. This is also called as pulse width modulation control (PWM).

Two cases with duty ratios, k as (a) 0.25 (25%), and (b) 0.75 (75%) are shown in the below figure. Hence, the output voltage can be varied by varying ON time, T_{ON} .

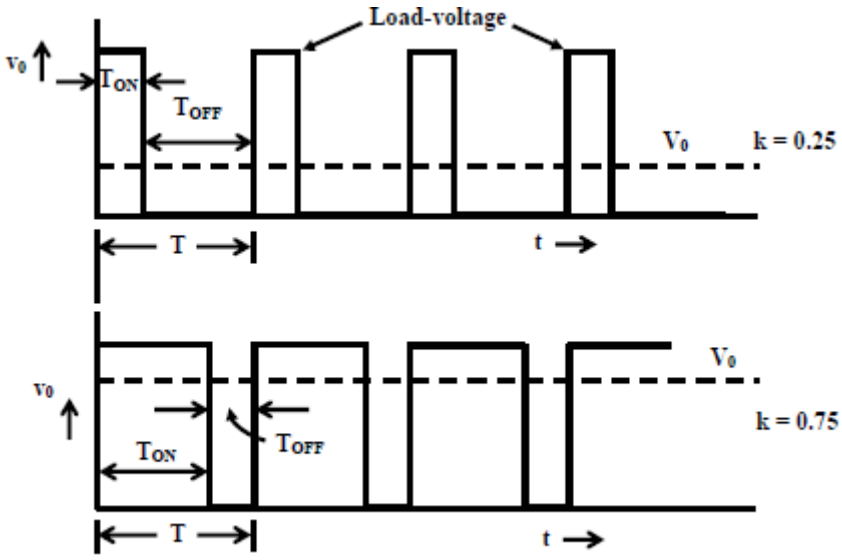
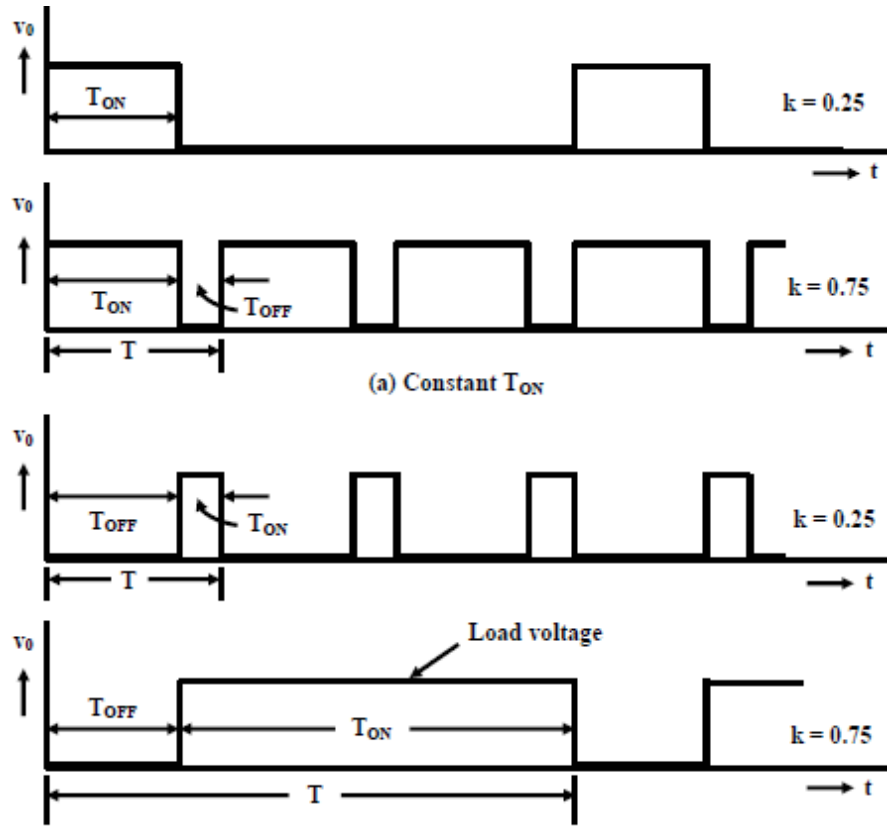


Fig. 17.4: Pulse-width modulation control (constant frequency)

Variable Frequency Operation

In this control strategy, the frequency (f = 1/T), or time period T is varied, keeping either (a) the ON time, T_{ON} constant, or (b) the OFF time, T_{OFF} constant.



(a) Constant T_{ON}

(b) Constant T_{OFF}

Fig. 17.5: Output voltage waveforms for variable frequency system

This is also called as frequency modulation control. Two cases with (a) the ON time, constant, and (b) the OFF time, constant, with variable frequency or time period are shown in below figure. The output voltage can be varied in both cases, with the change in duty ratio, k= T_{ON}/ T .

4.4 Different chopper configuration

(Single quadrant class A and class B, Two quadrant class C and class D & Four quadrant class E)

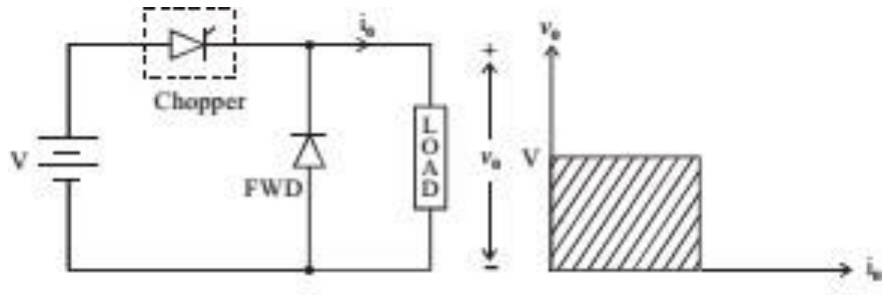
Classification Of Choppers

Depending on their operation Choppers are classified as follows.

1. Class A Chopper
2. Class B Chopper
3. Class C Chopper
4. Class D Chopper
5. Class E Chopper

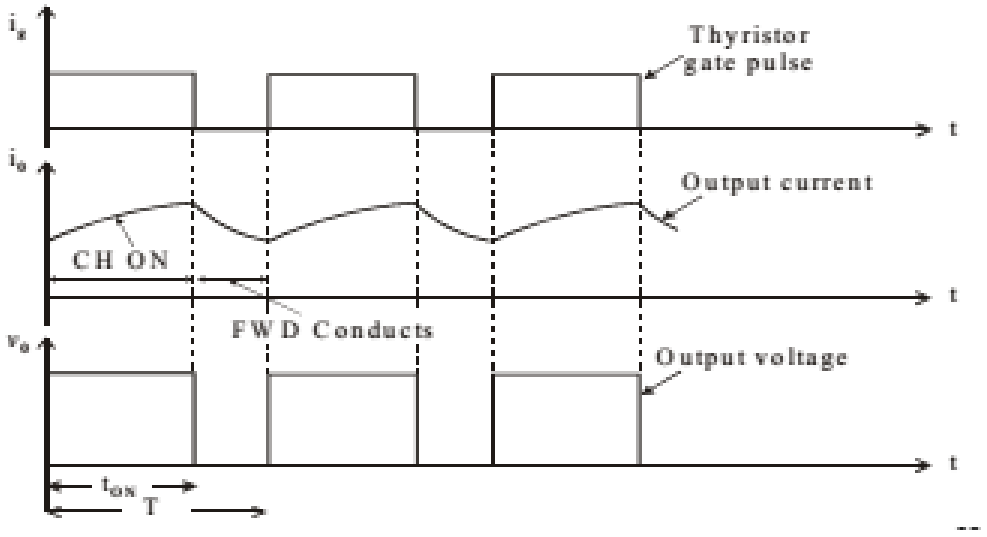
Single quadrant class A

When chopper is ON, supply voltage V is connected across the load. When chopper is OFF, v_O= 0 and the load current continues to flow in the same direction through the FWD (Freewheeling diode). The average values of output voltage and current are always positive. Class A Chopper is a step-down chopper in which power always flows form source to load.



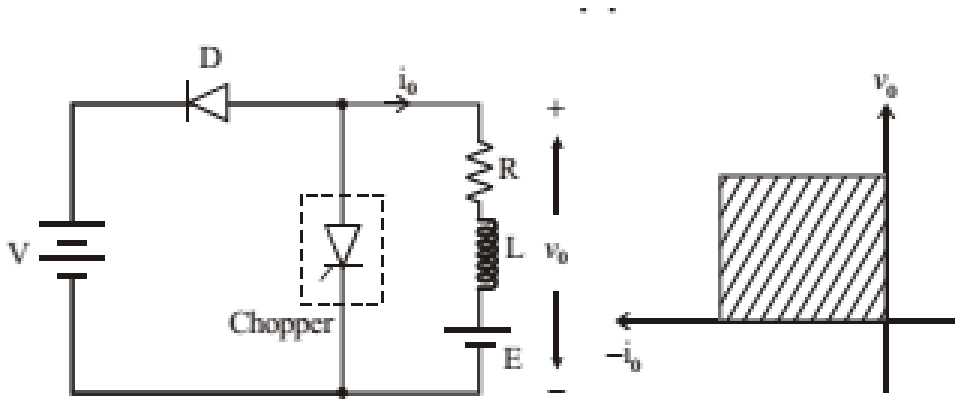
Class A Chopper is a first quadrant chopper .

It is used to control the speed of dc motor. The output current equations obtained in step down chopper with R-L load can be used to study the performance of Class A Chopper It is used to control the speed of dc motor. The output current equations obtained in step down chopper with R-L load can be used to study the performance of Class A Chopper



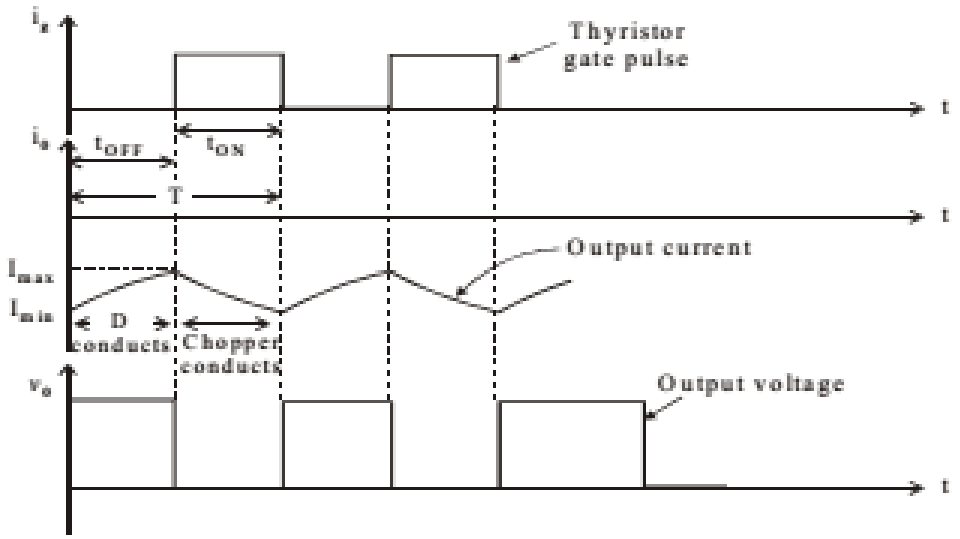
Second Quadrant Class B Chopper

When chopper is ON, E drives a current through L and R in a direction opposite to that shown in figure.



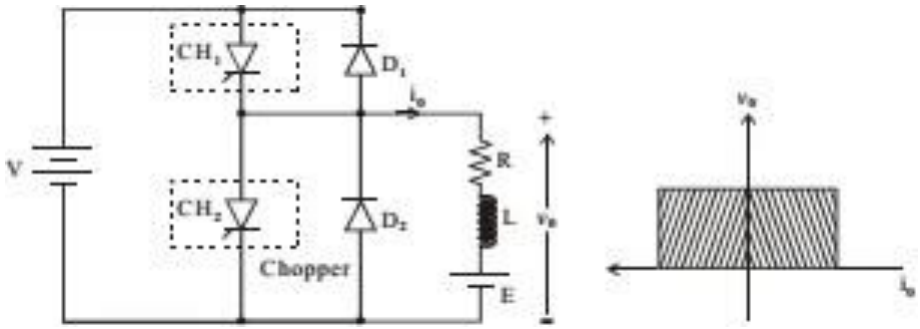
Class B Chopper operates in second quadrant

During the ON period of the chopper, the inductance L stores energy.When Chopper is OFF, diode D conducts, and part of the energy stored in inductor L is returned to the supply.Average output voltage is positive and average output current is negative. In this chopper, power flows from load to source. Class B Chopper is used for regenerative braking of dc motor. Class B Chopper is a step-up chopper.



Two Quadrant Class-C Chopper

Class C Chopper is a combination of Class A and Class B Choppers. For first quadrant operation, CH_1 is ON or D_2 conducts.

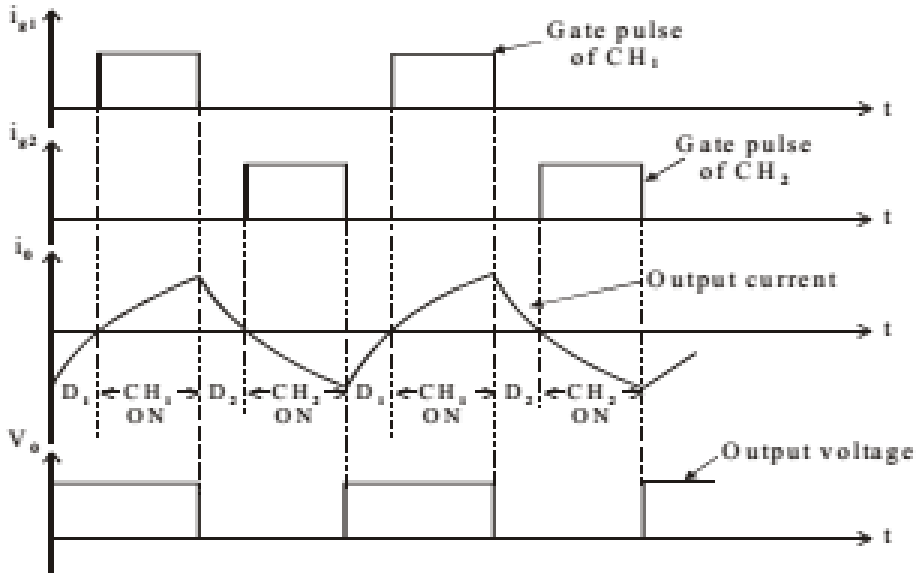


For second quadrant operation, CH_2 is ON or D_1 conducts. When CH_1

is ON, the load current is positive. The output voltage is equal to _V' & the load receives power from the source. When CH_1 is turned OFF, energy stored in inductance L forces current to flow through the diode D_2 and the output voltage is zero. Current continues to flow in positive direction.

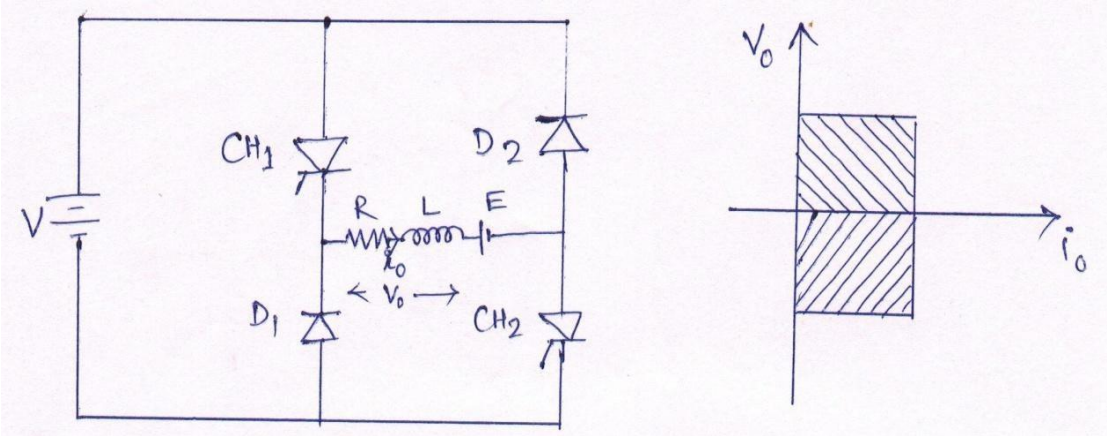
When CH_2 is triggered, the voltage E forces current to flow in opposite direction through L and CH_2. The output voltage is zero. On turning OFF CH_2, the energy stored in the inductance drives current through diode D_1 and the supply. Output voltage is V, the input current becomes negative and power flows from load to source. Average output voltage is positive. Average output current can take both positive and negative values. Choppers CH_1 & CH_2 should not be turned ON simultaneously as it would result in short circuiting the supply.

Class C Chopper can be used both for dc motor control and regenerative braking of dc motor. Class C Chopper can be used as a step-up or step-down chopper.

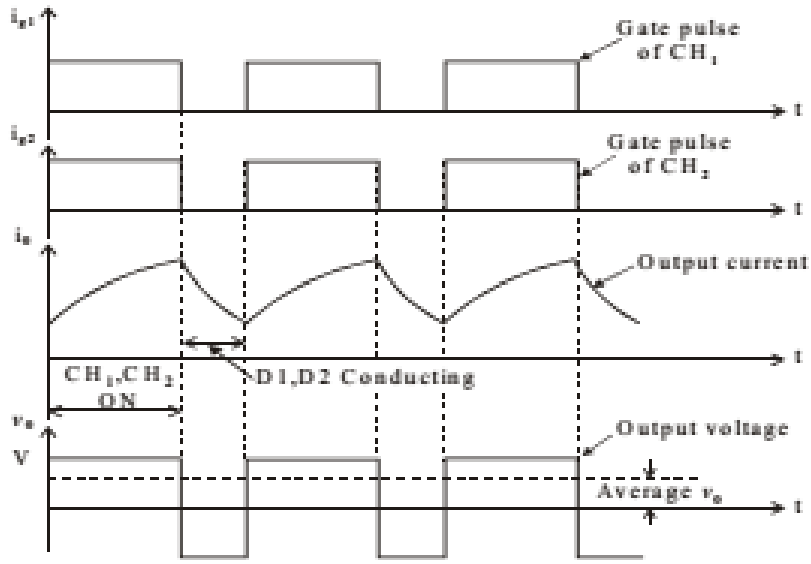


Two Quadrant Class-D Chopper

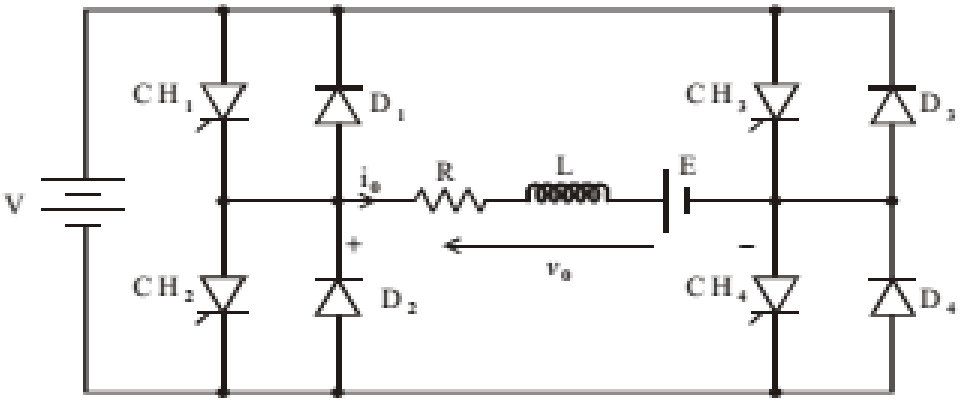
Class D is a two quadrant chopper.



When both $CH_1$and CH_2 are triggered simultaneously, the output voltage v_O = V and output current flows through the load. When CH_1 and CH_2 are turned OFF, the load current continues to flow in the same direction through load, D_1 and D_2 , due to the energy stored in the inductor L. Output voltage v_O = - V . Average load voltage is positive if chopper ON time is more than the OFF time. Average output voltage becomes negative if $t_{ON} < t_{OFF}$. Hence the direction of load current is always positive but load voltage can be positive or negative.

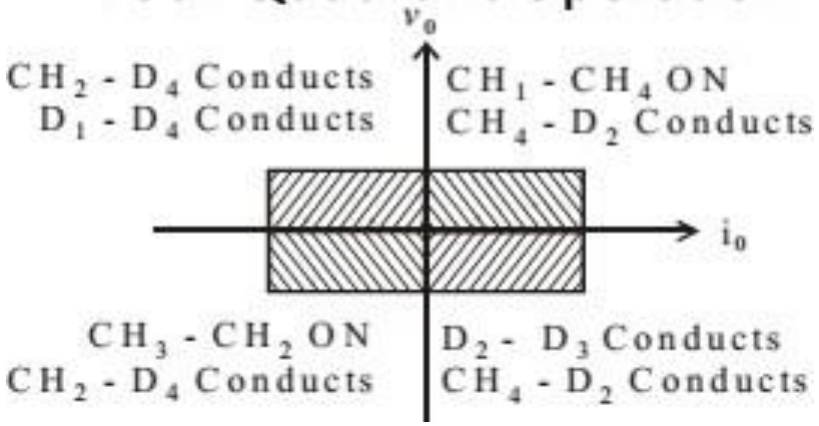


Four Quadrant Class-E Chopper



Class E is a four quadrant chopper. When CH_1 and CH_4 are triggered, output current i_O flows in positive direction through CH_1 and CH_4, and with output voltage $v_O = V$. This gives the first quadrant operation. When both CH_1 and CH_4 are OFF, the energy stored in the inductor L drives i_O through D_2 and D_3 in the same direction, but output voltage v_O. Therefore the chopper operates in the fourth quadrant. When CH_2 and CH_3 are triggered, the load current i_O flows in opposite direction & output voltage $v_O = -V$. Since both i_O and v_O are negative, the chopper operates in third quadrant. When both CH_2 and CH_3 are OFF, the load current i_O continues to flow in the same direction D_1 and D_4 and the output voltage $v_O = V$. Therefore the chopper operates in second quadrant as v_O is positive but i_O is negative.

Four Quadrant Operation



Chapter-5. Inverters

The word ‗inverter' in the context of power-electronics denotes a class of power conversion (or power conditioning) circuits that operates from a dc voltage source or a dc current source and converts it into ac voltage or current. The ‗inverter' does reverse of what ac-to-dc ‗converter' does (refer to *ac to dc converters*).

Inverter is a device which converts dc power to ac power at a desired output voltage and frequency (or at a desired current level and frequency).

5.1 Classification of inverters

Inverters can be broadly classified into two types, viz. voltage source inverter (VSI) and current source inverter (CSI).

According to the connection of semiconductor devices they are classified as (1) Bridge inverter (2) Series inverter and (3) Parallel inverter.

The nomenclature ‗inverter' is sometimes also used for ac to dc converter circuits if the power flow direction is from dc to ac side.

'Inverter' is referred as a circuit that operates from a stiff dc source and generates ac output. If the input dc is a voltage source, the inverter is called a voltage source inverter (VSI). Similarly a current source inverter (CSI) is one, where the input to the circuit is a current source.

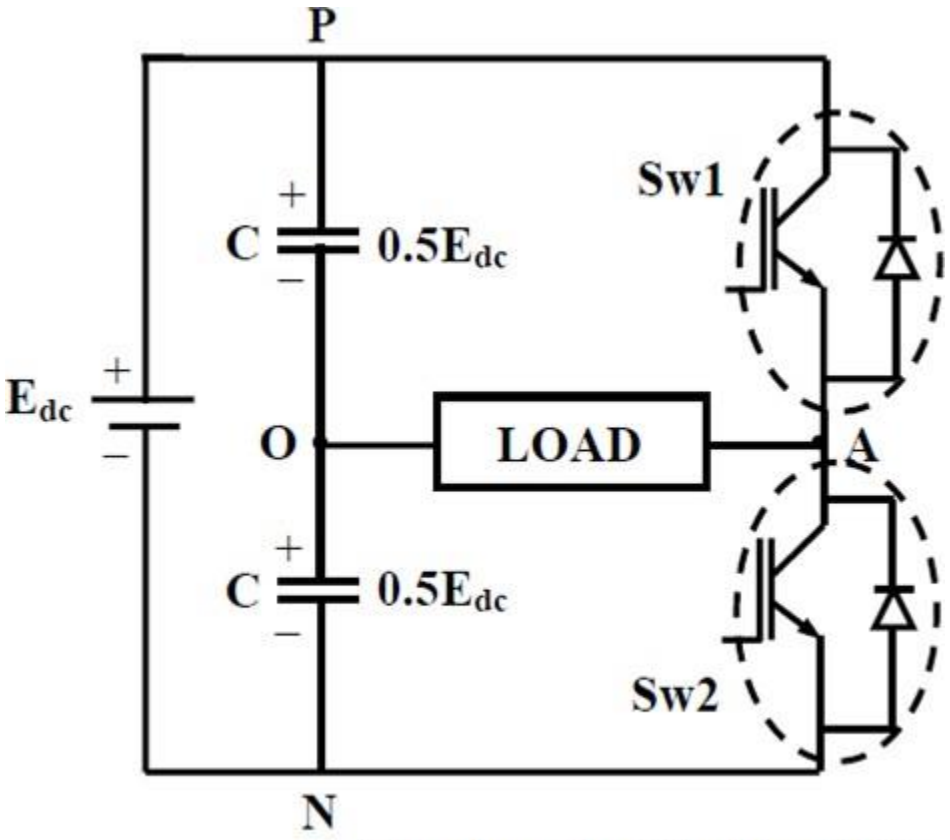
The VSI circuit has direct control over ‗output (ac) voltage' whereas the CSI directly controls ‗output (ac) current'. Shape of voltage waveforms output by an ideal VSI should be independent of load connected.

5.2 Single phase half bridge voltage source inverter

A single-phase square wave type voltage source inverter produces square shaped output voltage for a single-phase load. Such inverters have very simple control logic and the power switches need to operate at much lower frequencies compared to switches in some other types of inverters.

It is assumed that the input dc voltage (E_{dc}) is constant and the switches are lossless. In half bridge topology the input dc voltage is split in two equal parts through an ideal and loss-less capacitive potential divider. The half bridge topology consists of one leg (one pole) of switches whereas the full bridge topology has two such legs. Each leg of the inverter consists

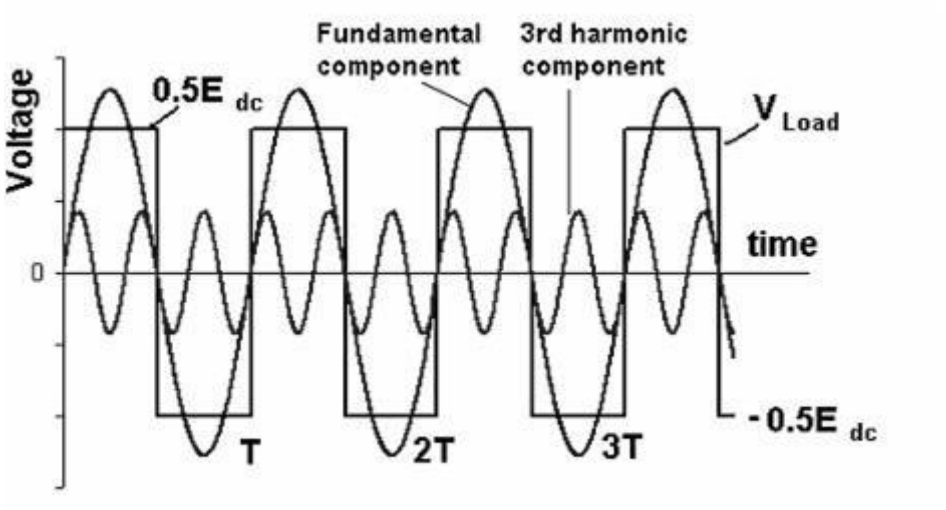
of two series connected electronic switches shown within dotted lines in the figures. Each of these switches consists of an IGBT type controlled switch across which an uncontrolled diode is put in anti-parallel manner.



A 1-phase half bridge VSI

These switches are capable of conducting bi-directional current but they need to block only one polarity of voltage. In half bridge topology the single-phase load is connected between the mid-point of the input dc supply and the junction point of the two switches (in Fig. above these points are marked as _O‘ and _A‘ respectively). For ease of understanding, the switches Sw1 and Sw2 may be assumed to be controlled mechanical switches that open and close in response to the switch control signal. Now, if the switches Sw1 and Sw2 are turned on alternately with duty ratio of each switch kept equal to 0.5, the load voltage (VAO) will be square wave with a peak-to-peak magnitude equal to input dc voltage (E_{dc}). Fig. shows a typical load voltage waveform output by the half bridge inverter. VAO acquires a magnitude of +0.5 E_{dc} when Sw1 is on and the magnitude reverses to -0.5 E_{dc} when Sw2 is turned on. The peak-to-peak magnitude of the fundamental frequency component of the square wave voltage, is equal to $4/\pi E_{dc}$. The two switches of the inverter leg are turned on in a complementary manner. For a general load, the switches should neither be simultaneously on

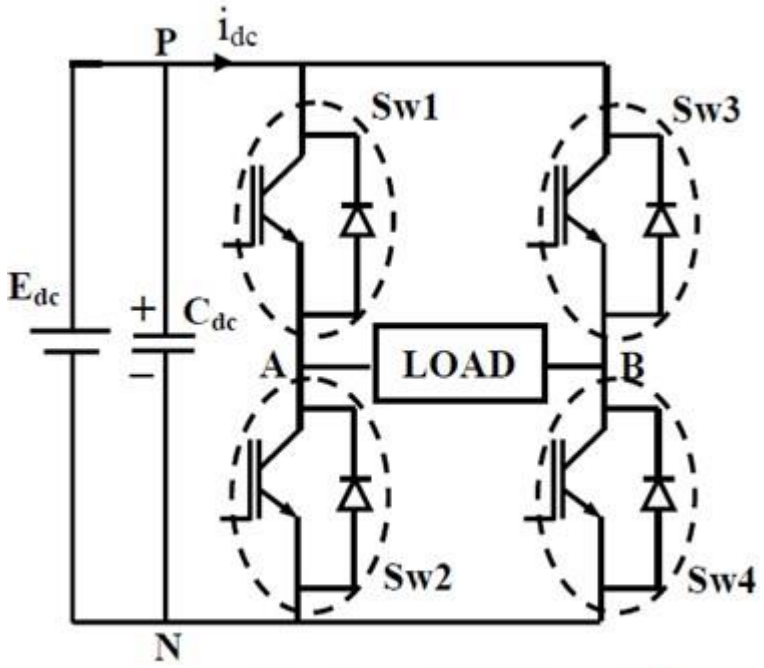
nor be simultaneously off. Simultaneous turn-on of both the switches will amount to short circuit across the dc bus and will cause the switch currents to rise rapidly.



Square wave load voltage output by half-bridge inverter

5.3 Single-Phase Full Bridge Inverter

The single-phase full bridge circuit (Fig. shown below) can be thought of as two half bridge circuits sharing the same dc bus.



A 1-phase full-bridge VSI

The full bridge circuit will have two pole-voltages (V_{AO} and V_{BO}), which are similar to the pole voltage V_{AO} of the half bridge circuit. Both V_{AO} and V_{BO} of the full bridge circuit are square waves but they will, in general, have some phase difference. Fig. shows these pole

voltages staggered in time by _t‘ seconds. It may be more convenient to talk in terms of the phase displacement angle _Φ‘ defined as below:

Φ = (2π) t/T Radians. ..... (i) ,

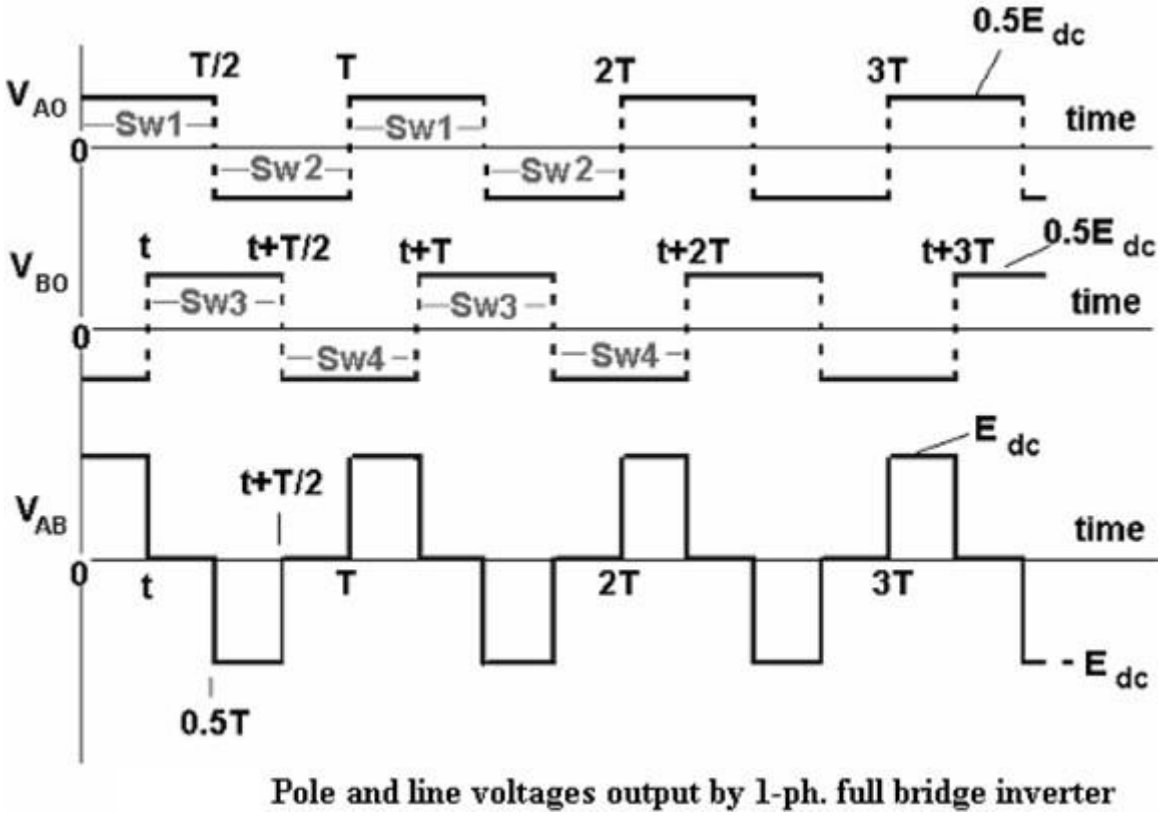
where _t‘ is the time by which the two pole voltages are staggered and _T‘ is the time period of the square wave pole voltages.

The pole voltage VAO of the full bridge inverter may again be written as in Eqn.(i), used earlier for the half bridge inverter. Taking the phase shift angle _Φ‘ into account, the pole-B voltage may be written as

$$V_{BO} = \sum_{n=1,3,5,7,\ldots,\infty} \frac{2E_{dc}}{n\pi} \sin n(wt - \Phi)$$

Difference of V_{AO} and V_{BO} gives the line voltage V_{AB}. In full bridge inverter the single phase load is connected between points _A‘ and _B‘ and the voltage of interest is the load voltage V_{AB}. Taking difference of the voltage expressions we get

$$V_{AB} = \sum_{n=1,3,5,7,\ldots,\infty} \frac{2E_{dc}}{n\pi} \left[\sin nwt - \sin n(wt - \Phi)\right]$$

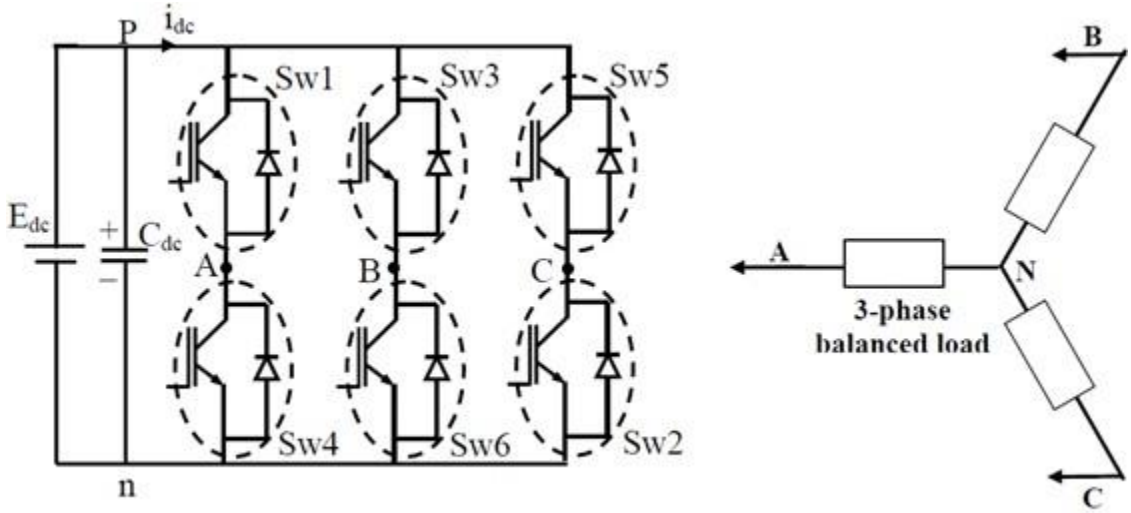


Pole and line voltages output by 1-ph. full bridge inverter

5.4 Three phase bridge inverter

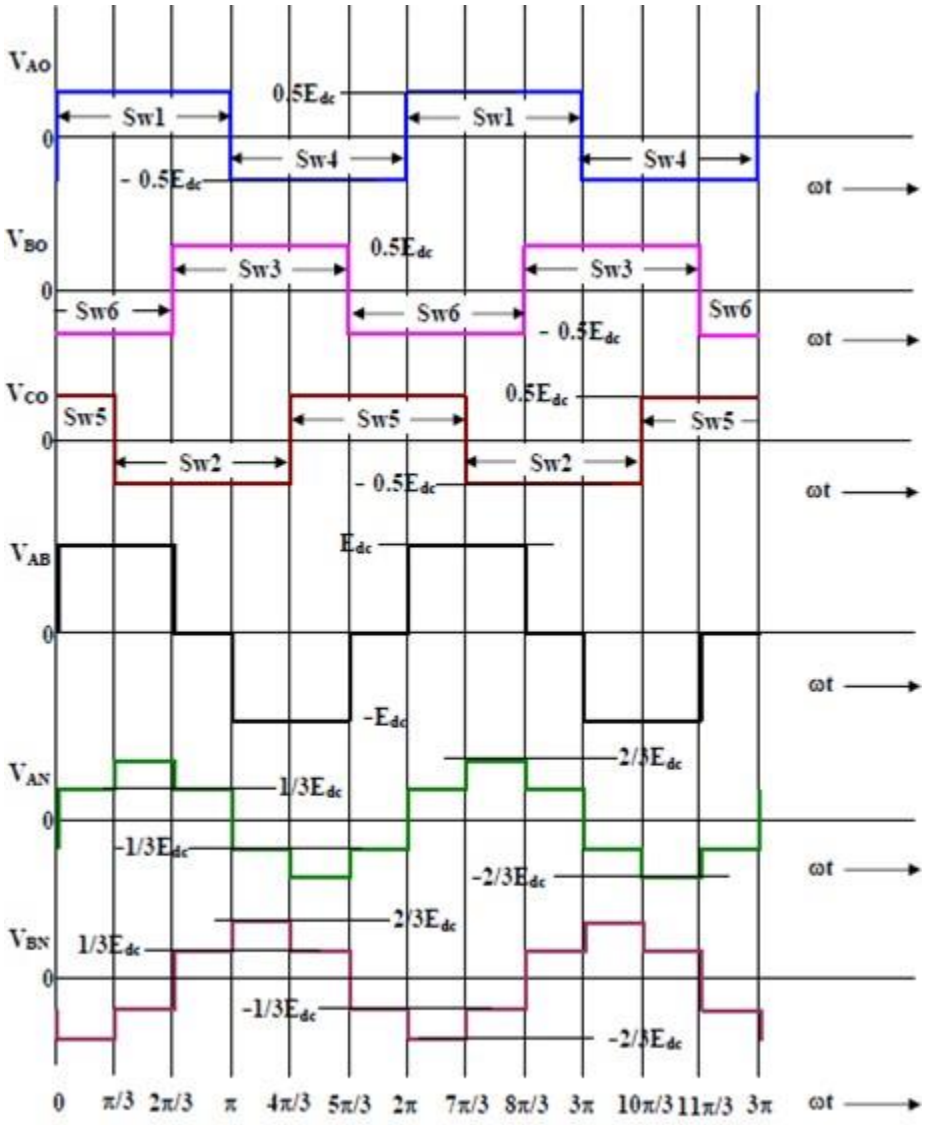
A 3-phase bridge type VSI with square wave pole voltages is described below. The output from this inverter is to be fed to a 3-phase balanced load. The below figure shows the power circuit of the three-phase inverter. This circuit may be identified as three single-phase half-bridge inverter circuits put across the same dc bus. The individual pole voltages of the 3-phase bridge circuit are identical to the square pole voltages output by single phase half bridge or full bridge circuits. The three pole voltages of the 3-phase square wave inverter are shifted in time by one third of the output time period.

It may be seen that with the chosen numbering the switches turn on in the sequence:- Sw1, Sw2, Sw3, Sw4, Sw5, Sw6, Sw1, Sw2,….and so on. Identifying the switching cycle time as 360 degrees (2π radians), it can be seen that each switch conducts for 180^0 and the turning on of the adjacent switch is staggered by 60 degrees. The upper and lower switches of each pole (leg) of the inverter conduct in a complementary manner. To reverse the output phase sequence, the switching sequence may simply be reversed.



A 3-phase Voltage Source Inverter (VSI) feeding a balanced load

Considering the symmetry in the switch conduction pattern, it may be found that at any time three switches conduct. It could be two from the upper group of switches, which are connected to positive dc bus, and one from lower group or vice-versa (i.e., one from upper group and two from lower group). According to the conduction pattern indicated in waveform diagram there are six combinations of conducting switches during an output cycle: - (Sw5, Sw6, Sw1), (Sw6, Sw1, Sw2), (Sw1, Sw2, Sw3), (Sw2, Sw3, Sw4), (Sw3, Sw4, Sw5), (Sw4, Sw5, Sw6). Each of these combinations of switches conducts for 60^0 in the sequence mentioned above to produce output phase sequence of A, B, C.



Some relevant voltage waveforms output by a 3-phase square wave VSI

5.5 Applications of inverter

Inverters are used in variable speed ac motor drives, induction heating, UPS (uninterruptible power supplies), stand-by air-craft power supplies, HVDC transmission line, regulated voltage and frequency power supply.

Chapter-6. CYCLOCONVERTER

The cyclo-converter is a type of power controller, where an alternating voltage at supply frequency is converted directly to an alternating voltage at load frequency (normally lower), without any intermediate dc stage.

Simply, it can be defined as a device that converts ac power at one frequency to ac power at a different frequency with single stage conversion.

6.1 Types of Cycloconverter

Depending on frequency cycloconverters are of two types, viz. Step-up cycloconverter and Step-down cycloconverter.

In step-up type cycloconverter the output frequency (f_0) is greater than the supply or input frequency (f_s) i.e. $f_0 > f_s$

In step-down type the output frequency is less than the input frequency, i.e. $f_0 < f_s$

Similarly depending on supply it is of 3 types, viz. 1-Φ to 1-Φ, 3-Φ to 3- Φ and 3-Φ to 1-Φ. Also depending on the type of connection it is of mid-point type or bridge type.

Applications of cycloconverter

Its various applications include speed control of high power ac drives, induction heating, static VAR compensation. Also used for converting variable speed alternator voltage to constant frequency output voltage for use as power supply in aircraft or chip-boards.

6.2 Advantages and Disadvantages of Cyclo-converter

Advantages

1. In a cycloconverter, ac power at one frequency is converted directly to a lower frequency in a single conversion stage.

2. Cycloconverter functions by means of phase commutation, without auxiliary forced commutation circuits. The power circuit is more compact, eliminating circuit losses associated with forced commutation.

3. Cycloconverter is inherently capable of power transfer in either direction between source and load. It can supply power to loads at any power factor, and is also capable of regeneration over the complete speed range, down to standstill. This feature makes it preferable for large reversing drives requiring rapid acceleration and deceleration, thus suited for metal rolling application.

4. Commutation failure causes a short circuit of ac supply. But, if an individual fuse blows off, a complete shutdown is not necessary, and cycloconverter continues to function with somewhat distorted waveforms. A balanced load is presented to the ac supply with unbalanced output conditions.

5. Cycloconverter delivers a high quality sinusoidal waveform at low output frequencies, since it is fabricated from a large number of segments of the supply waveform. This is often preferable for very low speed applications.

6. Cycloconverter is extremely attractive for large power, low speed drives.

Disadvantages

1. Large number of thyristors is required in a cycloconverter, and its control circuitry becomes more complex. It is not justified to use it for small installations, but is economical for units above 20 kVA.

2. For reasonable power output and efficiency, the output frequency is limited to one-third of the input frequency.

3. The power factor is low particularly at reduced output voltages, as phase control is used with high firing delay angle.

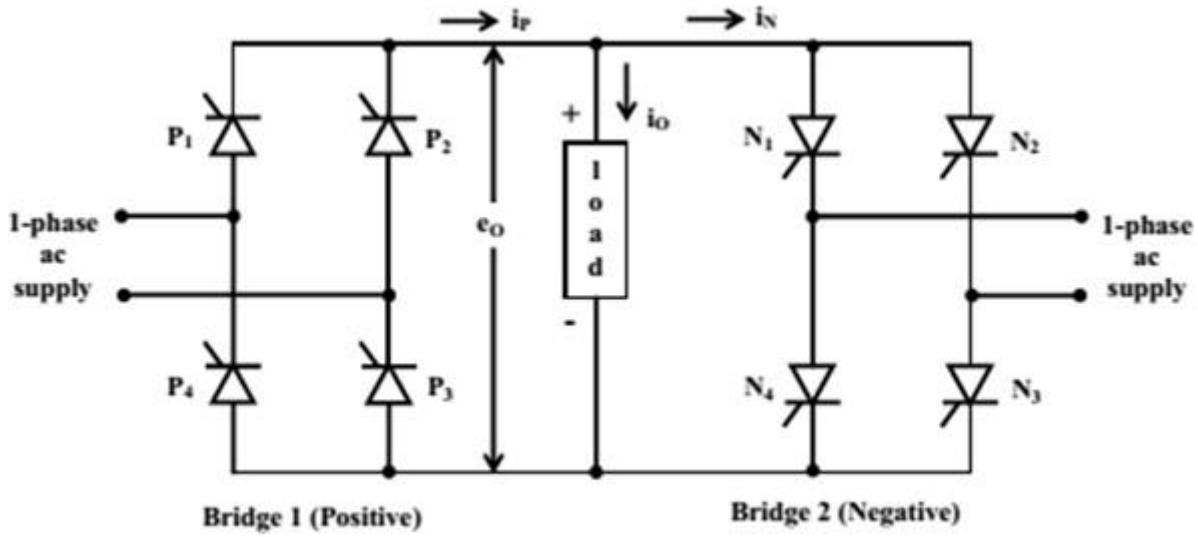
6.3 Operation of Single-phase to Single-phase Cyclo-converter

The circuit of a single-phase to single-phase cyclo-converter is shown in the below figure. Two full-wave fully controlled bridge converter circuits, using four thyristors for each bridge, are connected in opposite direction (back to back), with both bridges being fed from ac supply (50 Hz). Bridge 1 (P – positive) supplies load current in the positive half of the output cycle, while bridge 2 (N – negative) supplies load current in the negative half. The two bridges should not conduct together as this will produce short-circuit at the input. In this case, two thyristors come in series with each voltage source.

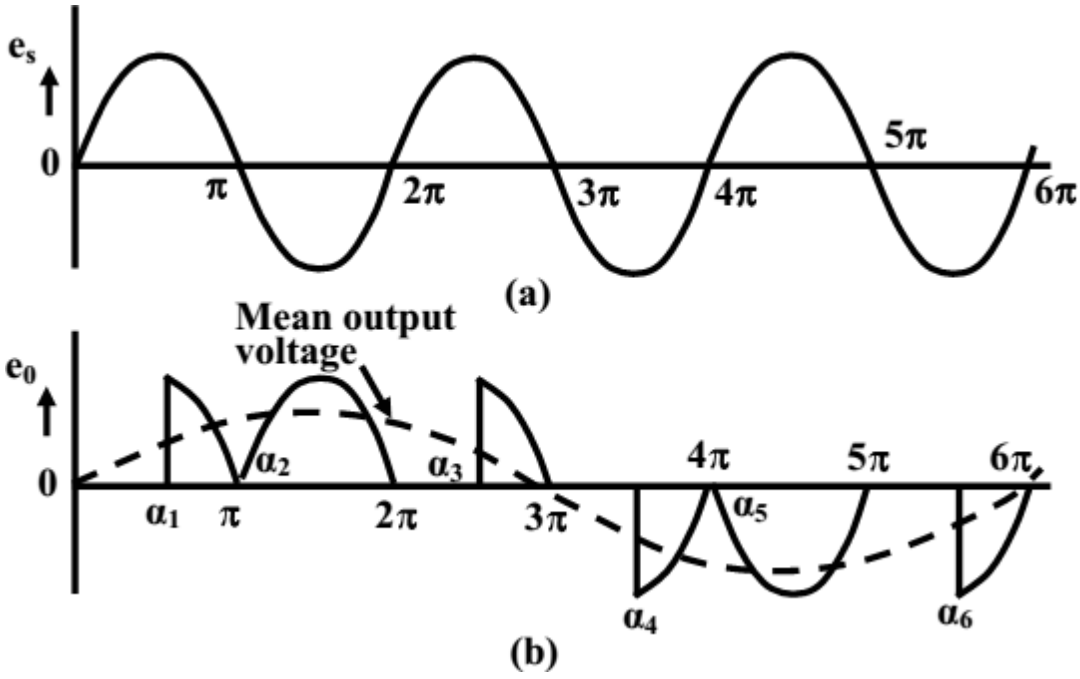
Resistive (R) Load:

For this load, the load current (instantaneous) goes to zero, as the input voltage at the end of each half cycle (both positive and negative) reaches zero (0).

Thus, the conducting thyristor pair in one of the bridges turns off at that time, i.e. the thyristors undergo natural commutation. So, operation with discontinuous current takes place(as shown in the waveform), as current flows in the load, only when the next thyristor pair in that bridge is triggered, or pulses are fed at respective gates. Taking first bridge 1 (positive), and assuming the top point of the ac supply as positive with the bottom point as negative in the positive half cycle of ac input, the odd numbered thyristor pair, P_1& P_3 is triggered after phase delay (α_1), such that current starts flowing through the load in this half cycle. In the next (negative) half cycle, the other thyristor pair (even-numbered), P_2& P_4in that bridge conducts, by triggering them after suitable phase delay from the start of zero-crossing. The current flows through the load in the same direction, with the output voltage also remaining positive. This process continues for one more half cycle (making a total of three) of input voltage (=f_1 50 Hz).



Single-phase to single-phase cycloconverter (using thyristor bridges)



To obtain negative output voltage, in the next three half cycles of input voltage, bridge 2 is used. Following same logic, if the bottom point of the ac supply is taken as positive with the top point as negative in the negative half of ac input, the odd-numbered thyristor pair, N_1& N_3 conducts, by triggering them after suitable phase delay from the zero-crossing. Similarly, the even-numbered thyristor pair, N_2& N_4 conducts in the next half cycle.

Both the output voltage and current are now negative. As in the previous case, the above process also continues for three consecutive half cycles of input voltage.

Chapter-7 Protection, Ratings & failure of Power Electronics Devices

7.1 Give specification, ratings and nomenclature of Thyristors

The performance of an SCR is affected by the junction temperature, because of change in carrier densities in the four layers and the junction temperature naturally depends upon the internal power losses of the device and the efficiency of heat transfer mechanism. The factors contributing toward rise in junction temperature are

- On-state voltage drop across the device (SCR),
- Leakage current in the blocking or off state and
- Power dissipation at gate.

There are three types of ratings for an SCR like continuous; repetitive and non-repetitive. Because the SCR has a short thermal time constant, there is no difference between continuous and intermittent ratings above a few second conduction period.

(a) Continuous Current Ratings.

Continuous current ratings of SCRs are normally given in terms of average or rms values depending upon whether the device is unilateral or bilateral. However, rms current rating is more commonly used in the rating procedure for a device. The rms current rating of the device is useful, because it is essentially independent of the conduction angle, whereas the average current rating decreases with the decrease in conduction angle. Also, the rms current rating of the device is larger than the average current rating. This rms current flows through the conductive part of the lead assembly, the device wiring and internal assembly parts and raises the temperature. The rms current rating must be limited to a safe value to prevent excessive heating in the resistive elements of the SCR, such as joints, leads etc. The rms current rating is also important when SCRs are used to supply large peak current to a load with low duty cycle.

(b) Repetitive Overload Current Ratings.

It is very common for rectifier equipment to frequently run on over-load. Though the duration of over-load is short, it is repetitive. It is quite obvious that the peak allowable junction temperature is never to be exceeded under any condition. So, the magnitude, duration and repetitive frequency of the overload current of the device should be such that under no case the peak allowable junction temperature is exceeded. This again depends on the thermal

resistance and transient thermal impedances of the device and the type and size of the heat sink. It also depends on the method of cooling (i.e. natural air cooling or forced air cooling), the velocity of cooling air, ambient temperature etc.

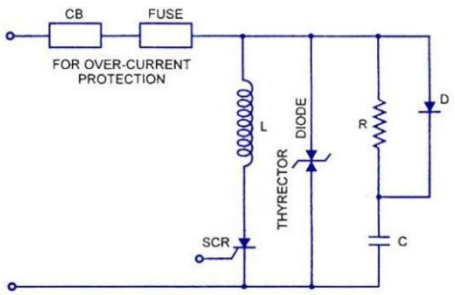
(c) Non-repetitive Surge Current Ratings.

Non-repetitive surge current ratings of the SCRs are provided by the manufacturer. Such surge current is assumed to be imposed on the device when it is operating at the maximum rated voltage, current and temperature condition in a half-wave circuit delivering a resistive load. These ratings are such that during the surge current, the maximum repetitive junction temperature of the device may be exceeded. During this brief period, the forward blocking capability of the device is lost until the device is cooled down to or below the maximum rated operating temperature. The surge current is not a regular feature of the device and occurs during severe fault condition. These ratings provide the instantaneous over-load capacity of the device and are used in designing the protective devices for it. Such ratings are usually provided in terms of non-recurring surge current with respect to time duration of occurrence and I^2t. The maximum surge current rating is provided for minimum time duration of one half cycle of the supply frequency, i.e. 10 ms; for the supply frequency of 50 Hz. I^2t ratings apply for non-repetitive surge overloads shorter than one half cycle. At this condition SCR behaves like a resistor with a fixed thermal capacity. The heat dissipation during the small period is negligible. I^2t rating of the device represents the capability of the device to withstand the overload current for the specified time. The current is rms value for the time interval t.

7.2 Over voltage and over current protection of SCR

SCRs are sensitive to **high voltage**, **over-current**, and any form of transients. For satisfactory and reliable operation they are required to be protected against such abnormal operating conditions. Because of complex and expensive protection, usually some margin is provided in the equipment by selecting devices with ratings higher (3 or 4 times higher) than those required for normal operation. But it is always not economical to use devices of higher ratings, hence their protection is imperative.

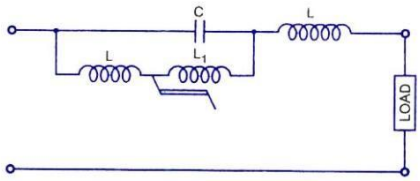
Over-voltage Protection.



Over-voltage Protection

High forward voltage protection is inherent in SCRs. The SCR will breakdown and start conducting before the peak forward voltage is attained so that the high voltage is transferred to another part of the circuit (usually the load). The **turn-on of SCR** causes a large current to flow and poses a problem of over-current protection.

Over-current Protection.



Over-current Protection

Over-current protection can be provided by connecting a circuit breaker and a fuse in series with the SCR, as usually done for the protection of any circuit. However, there are some reservations to their use. A semiconductor device is capable of taking overloads for a limited period, so the fuse used should have high breaking capacity and rapid interruption of current. There must be a similarity of SCR and fuse I^2t rating without developing high voltage transients which endanger those SCRs in the off or infinite impedance condition. These are contradictory requirements necessitating voltage protection when fast-acting fuses are employed. Fuses when used, their arc voltages are kept below 1.5 times the peak circuit voltage. For small power applications it is pointless to employ high speed fuses for circuit protection because it may cost more than the SCR. Current magnitude detection can be employed and is used in many applications. When an over-current is detected the gate circuits are controlled either to **turn-off the appropriate SCRs**, or in phase commutation, to reduce the conduction period and so the average value of the current.

If the output to the load from the **SCR circuit** is alternating current, LC resonance provides over-current protection as well as filtering. A current limiting device employing a saturable reactor is shown in figure. With normal currents the saturable reactor L_1 offers high impedance and C and L are in series resonance to offer zero impedance to the flow of current

of the fundamental harmonic. An over-current saturates L_1 and so gives negligible impedance. There is LC parallel resonance and hence infinite impedance to the flow of current at the resonant frequency.

7.3 dv/dt and di/dt protection of SCR

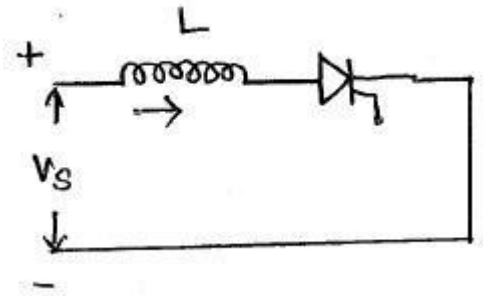
- For reliable operation of SCR, it should be operated within the specific ratings.
- SCRs are very delicate devices and so they must be protected against abnormal operating conditions. Various protection of SCR are

di/dt Protection

dv/dt Protection

di/dt Protection:-

- di/dt is the rate of change of current in a device.
- When SCR is forward biased and is turned ON by the gate signal, the anode current flows.
- The anode current requires some time to spread inside the device. (Spreading of charge carriers)
- But if the rate of rise of anode current (di/dt) is greater than the spread velocity of charge carriers then local hot spots is created near the gate due to increased current density. This localised heating may damage the device.
- Local spot heating is avoided by ensuring that the conduction spreads to the whole area very rapidly. (OR) The di/dt value must be maintained below a threshold (limiting) value.
- This is done by means of connecting an inductor in series with the thyristor.

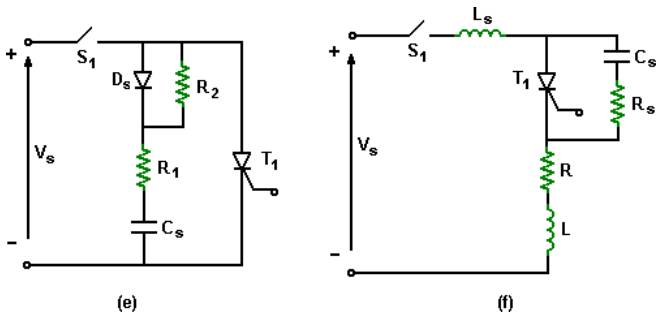


- The inductance L opposes the high di/dt variations.
- When the current variation is high, the inductor smooths it and protects the SCR from damage. (Though di/dt variation is high, the inductor 'L' smooths it because it takes some time to charge). $L \geq [Vs / (di/dt)]$

dv/dt Protection:-

- dv/dt is the rate of charge of voltage in SCR.

- We know that i_C=C.dv/dt. ie, when dv/dt is high, i_C is high.
- This high current(i_C) may turn ON SCR even when gate current is zero. This is called as dv/dt turn ON or false turn ON of SCR.

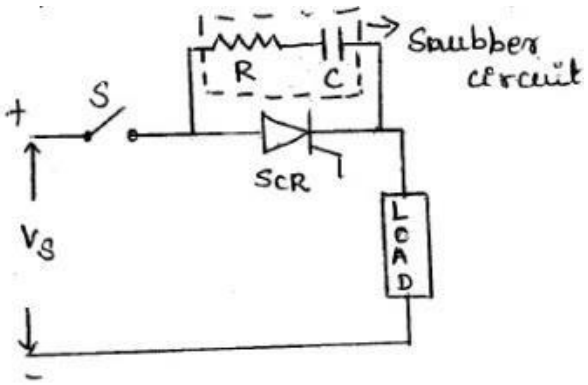


It is sometimes necessary to use one resistor for dv/dt and another for limiting the discharge current of the snubber capacitor. This arrangement is shown in figure (e). In this circuit, $\mathbf{R}_1$ and $\mathbf{C}_S$ are used for dv/dt protection, while $\mathbf{R}_1$ + $\mathbf{R}_2$ is used for limiting the capacitor discharge current.

The load can also be placed in series with the snubber components as shown in figure (f).

7.4 SNUBBER CIRCUIT:-

To protect the thyristor against false turn ON or against high dv/dt a "Snubber Circuit" is used.



- The snubber Circuit is a series combination of resistor 'R' and capacitor 'C'.
- They are connected across the thyristor to be protected.
- The capacitor 'C' is used to limit the dv/dt across the SCR.
- The resistor 'R' is used to limit high discharging current through the SCR.
- When switch S is closed, the capacitor 'C' behaves as a short-circuit.
- Therefore voltage across SCR is zero.
- As time increases, voltage across 'C' increases at a slow rate.

- Therefore dv/dt across 'C' and SCR is less than maximum dv/dt rating of the device.
- The capacitor charges to full voltage Vs; after which the gate is triggered, and SCR is turned ON and high current flows through SCR.
- As di/dt is high, it may damage the SCR.To avoid this, the resistor R in series with 'C' will limit the magnitude of di/dt.
- The technique of 'snubbing' can apply to any switching circuit, not only to thyristor/triac circuits.
- The rate of rise of turn-off voltage is determined by the time constant R_LC. Where R_L is the circuit minimum load resistance, for instance the cold resistance of a heater or lamp, the winding resistance of a motor or the primary resistance of a transformer.

7.5 Describe the process involved in selecting an SCR for a particular application

The voltage and current ratings are important before selecting an SCR for a particular application. The voltage ratings of SCRs rare given for both stead-state and transient operation and for both forward and reverse blocking conditions. Consideration must be given to:

- Load Voltage - AC or DC, Line Voltage.
- Load Current - AC or DC, Max and Min.
- Input Voltage - AC or DC, Max and Min.
- Ambient Temperature - Required for Derating and heatsink calculations.
- Mounting Style - PCB, Chassis or DIN Rail Mounting
- International Approvals - UL, CSA, VDE, TUV, etc.

7.6 Reliability of SCR and mean time between failures (MTBF)

As a silicon semiconductor device, the SCR is compact, static, capable of being passivated and hermetically sealed, silent in operation and free from the effects of vibration and shock. A properly designed and fabricated SCR *has no inherent failure mechanism*. When properly chosen and protected, it should *have virtually an operating life without limits*, even in harsh atmosphere. Consequently, countless billions of operations can be expected, even in explosive and corrosive environments. All components — including power semiconductors — have the potential of failing or degrading in ways that could impair the proper operation of such systems. Well-known circuit techniques (including fusing and self-checking) are available to protect against the effects of such phenomena. For any systems where *safety* is in question fault analysis is recommended.

Mean Time Between Failures (MTBF)

Calculating Mean Time Before Failure (MTBF) for a solid state relay is, at best, a tricky proposition. Unlike a typical electromechanical relay, there are several variables that will directly impact the life expectancy of a solid state relay in a given application. These variables primarily revolve around the electrical characteristics of the application, such as load current, the duty-cycle of the load, the ambient temperature inside the panel, surge currents, etc. However, mechanical issues such as the mounting method, available airflow, and thermal interface between the relay and the panel / heat sink also impact the relay's life expectancy.

Therefore, Crydom does not publish a "fixed" MTBF specification. Instead, we provide an estimated MTBF specification range based on historical observation. That is, we calculate the MTBF by taking the total in-service hours over the previous two-year period and dividing that by the number of returns we have received from the field over the same period of time (solid state relays that were misapplied by the customer are not considered in the calculation). "In-service hours" is simply calculated by taking the number of products shipped over the specified period and assuming that they were in operation for eight hours per day over a five day work week. Then, to ensure that we maintain an adequate margin of error, we assume that only 10% of all field failures are returned to us for analysis and adjust the results accordingly.

The final result yields a MTBF rating of between 2 million and 40 million hours, depending upon the product family. However, for the sake of simplicity we state that the MTBF rating for our solid state relays is >2 million hours.

MTBF - or Mean Time Between Failures is calculated in hrs and is a prediction of a solid state relays reliability. MTBF = 1/λ (failure rate)

7.7 The three failures of an SCR (Mechanical, Electrical and Thermal)

Mechanical

- Auxiliary Cathode and Gate Leads not Twisted
- If the auxiliary cathode (small red) and gate (white) are not twisted together properly it can cause false triggering or the device turning on when it should be off. The proper twist for these is one twist per inch. This eliminates EMF (a.k.a. noise).
- Loose gate connection at SCR or terminal board.
- This is typically caused by improper or non-soldered gate connection to the device and/or firing board. It could also be the result of improper matching of connectors. That is,

metal or plastic undersized male connector fitting into female connector. There were incidences when they used 3/16‖ male with ¼‖ female. This will create heat (40 volt potential), which in turn melts solder to the terminal board and breaks the connection.

- Bad snubber (R&C) network across SCR.

- Snubbers are resistor capacitor networks (circuits) which limit rapid rises in voltage or current in short time periods. If the snubber network is malfunctioning or not designed to handle the load (as some of the older units did), spikes can be passed on to the SCR causing failure.

Electrical

- Cold solder joint on either the gate drive circuit or the snubber network are suspect to poor connections. Again, it boils down to getting good connections, avoiding heat build up and making sure there are no spurious paths for the current to take.

- Bad firing amplifier.

- A SCR may show that it is not conducting when it should be. This may be caused by insufficient, or no gate drive caused by a bad firing amplifier.

- Small crack in the printed circuit board electrical circuit.

- One of the more frustrating and hard to find problems is a small crack in the printed circuit board circuitry. This shows up as an intermittent in the system and therefore is difficult to trace.

Thermal

- Loss of cooling.

- The system cooling can either be liquid or air in conjunction with a pump and/or fan. If the cooling system fails, from clogged filter, loss of coolant pressure, or airflow, then the entire circuit is in danger. Significant heat is generated by these components and overheating will eventually cause junctions to start failing.

- Insufficient gate drive to the SCR.

- SCR‘s need a hard drive to get the total junction on and ready to accept the system current. A hard drive is typically an initial gating pulse of 25 volts at 1 amp for 1 microsecond then rapidly decaying to 3 volts and 500 milliamps. If the gate drive is insufficient to get the total junction on thin when the system current pulse occurs it will hit the portion of the junction that is on. This can cause a current burn through destroying the junction thus causing a device failure.

- Cracked Insulation.

- Old insulation that has become cracked can cause a short circuit under normal operating conditions. This will cause massive failure of electronic components including the SCR.
- In summary, SCR‘s will not fail by themselves. Something external causes them to fail. Before you pullout the failed SCR‘s and install new ones make sure you locate the cause of the failure. Check the above ten possibilities. If you still don‘t know the reason, have the failed devices analyzed to see if the junctions will give you an indication of the failure mode.

Chapter-8 Industrial Electronics

8.1 Power Supplies, Stabilizers and Generation voltage regulators

Power Supplies

A power supply is an electronic device that supplies electric energy to an electrical load. The primary function of a power supply is to convert one form of electrical energy to another and, as a result, power supplies are sometimes referred to as electric power converters. Some power supplies are discrete, stand-alone devices, whereas others are built into larger devices along with their loads. Examples of the latter include power supplies found in desktop computers and consumer electronics devices.

Every power supply must obtain the energy it supplies to its load, as well as any energy it consumes while performing that task, from an energy source. Depending on its design, a power supply may obtain energy from various types of energy sources, including electrical energy transmission systems, energy storage devices such as a batteries and fuel cells, electromechanical systems such as generators and alternators, solar power converters, or another power supply.

All power supplies have a power input, which receives energy from the energy source, and a power output that delivers energy to the load. In most power supplies the power input and output consist of electrical connectors or hardwired circuit connections, though some power supplies employ wireless energy transfer in lieu of galvanic connections for the power input or output. Some power supplies have other types of inputs and outputs as well, for functions such as external monitoring and control.

Types

DC power supply

AC-to-DC supply

Linear regulator

AC power supplies

Switched-mode power supply

Programmable power supply

Uninterruptible power supply

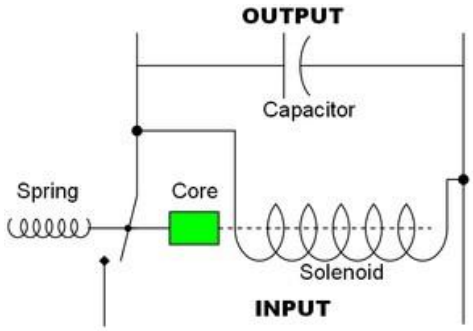
High voltage power supply

Generation voltage regulators

In electrical engineering, particularly power engineering, **voltage regulation** is a measure of change in the voltage magnitude between the sending and receiving end of a component, such as a transmission or distribution line. Voltage regulation describes the ability of a system to provide near constant voltage over a wide range of load conditions. The term may refer to a passive property that results in more or less voltage drop under various load conditions, or to the active intervention with devices for the specific purpose of adjusting voltage.

A **voltage regulator** is designed to automatically maintain a constant voltage level. A voltage regulator may be a simple "feed-forward" design or may include negative feedback control loops. It may use an electromechanical mechanism, or electronic components. Depending on the design, it may be used to regulate one or more AC or DC voltages.

Electronic voltage regulators are found in devices such as computer power supplies where they stabilize the DC voltages used by the processor and other elements. In automobile alternators and central power station generator plants, voltage regulators control the output of the plant. In an electric power distribution system, voltage regulators may be installed at a substation or along distribution lines so that all customers receive steady voltage independent of how much power is drawn from the line.



Types

Electronic voltage regulators

Electromechanical regulators

Automatic voltage regulator

Stabilizers

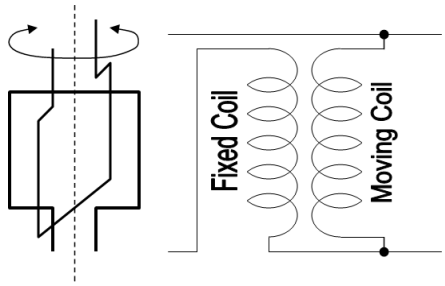
It is the type of voltage regulator used as generation of voltage regulation it may be of two types A.C voltage stabilizers and D.C voltage stabilizers.

A.C voltage stabilizers

This is an older type of regulator used in the 1920s that uses the principle of a fixed-position field coil and a second field coil that can be rotated on an axis in parallel with the fixed coil, similar to a variocoupler.

When the movable coil is positioned perpendicular to the fixed coil, the magnetic forces acting on the movable coil balance each other out and voltage output is unchanged. Rotating the coil in one direction or the other away from the center position will increase or decrease voltage in the secondary movable coil.

This type of regulator can be automated via a servo control mechanism to advance the movable coil position in order to provide voltage increase or decrease. A braking mechanism or high ratio gearing is used to hold the rotating coil in place against the powerful magnetic forces acting on the moving coil.



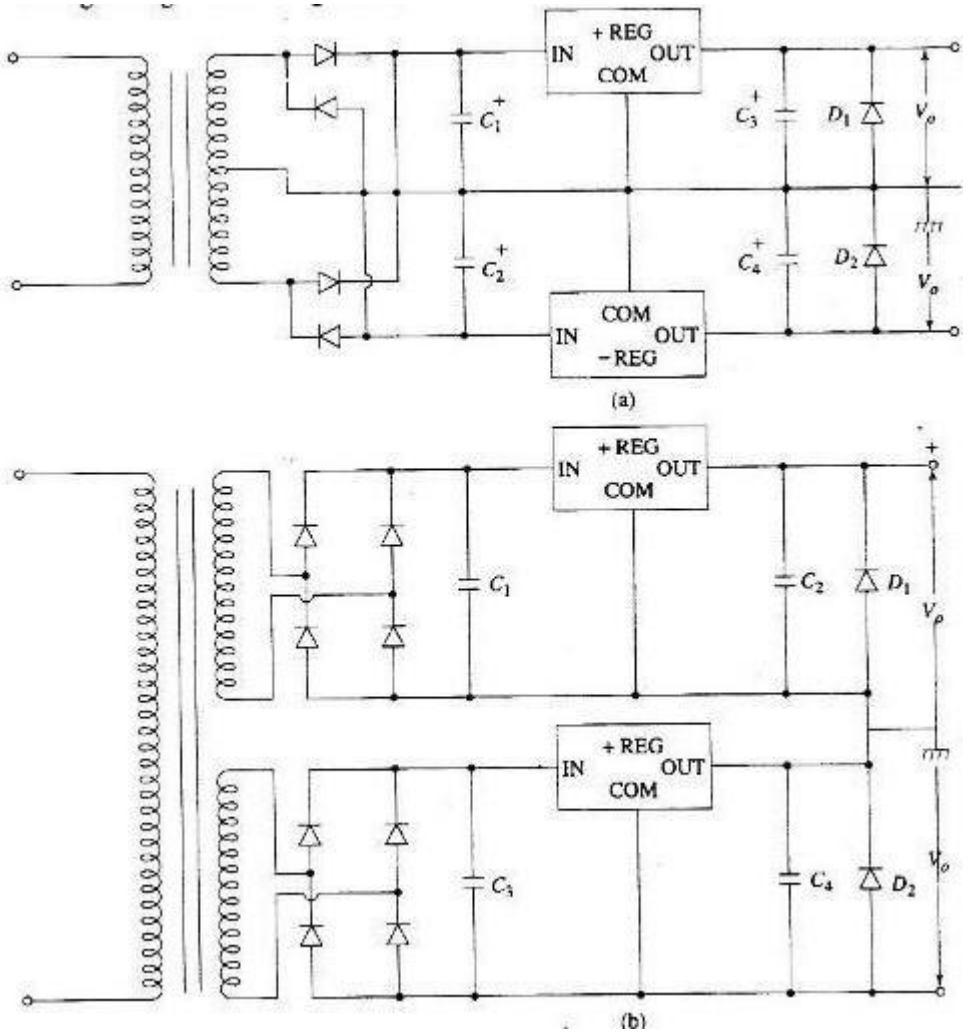
DC voltage stabilizers

Many simple DC power supplies regulate the voltage using either series or shunt regulators, but most apply a voltage reference using a shunt regulator such as a Zener diode, avalanche breakdown diode, or voltage regulator tube. Each of these devices begins conducting at a specified voltage and will conduct as much current as required to hold its terminal voltage to that specified voltage by diverting excess current from a non-ideal power source to ground, often through a relatively low-value resistor to dissipate the excess energy. The power supply is designed to only supply a maximum amount of current that is within the safe operating capability of the shunt regulating device.

If the stabilizer must provide more power, the shunt regulator output is only used to provide the standard voltage reference for the electronic device, known as the voltage stabilizer. The voltage stabilizer is the electronic device, able to deliver much larger currents on demand.

8.2 Schematic diagram of linear power supply that provides + or – 5V and + or -15V & its operation

The simplest dual non-tracking regulator requires +ve & -ve non –regulated power supply and one three terminal +ve & -ve IC regulator. The dual unregulated DC supply may be obtained from a transformer having a centre taped secondary and two full-wave rectifiers Fig-a, a transformer having two secondary and two bridge rectifiers Fig-b.



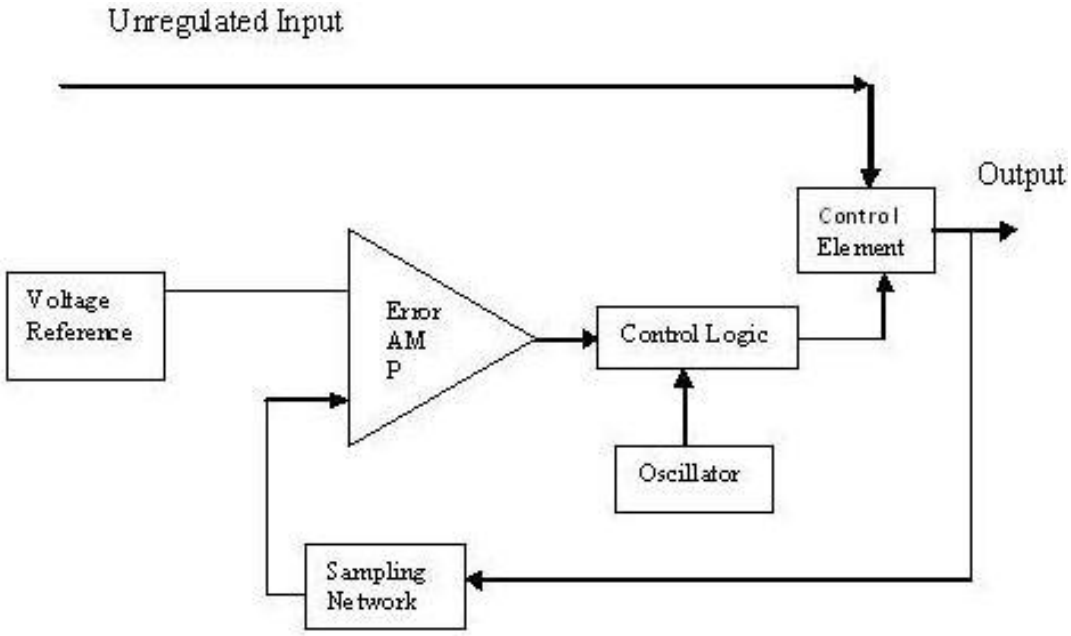
8.3 Schematic diagram of switched mode power supply (SMPS) and its operation & application

SMPS (Switched Mode Power Supply)

D.C. to D.C. converters and D.C. to A.C. Converters belong to the category of **Switched Mode Power Supplies (SMPS).** The various types of voltage regulators, used in Linear Power Supplies (LPS), fall in the category of dissipative regulator, as they have a

voltage control element usually transistor or zener diode which dissipates power equal to the voltage difference between an unregulated input voltage and a fixed supply voltage multiplied by the current flowing through it. The switching regulator acts as a continuously variable power converter and hence its efficiency is negligibly affected by the voltage difference. Hence the switching regulator is also known as _non-dissipative regulator‘. In a SMPS, the active device that provides regulation is always operated in cut-off or in saturation mode.

The input D.C. Supply is chopped at a higher frequency around 15 to 50 kHz using an active device like the BJT, power MOSFET or SCR and the converter transformer. Here the size of the ferrite core reduces inversely with the frequency. The lower limit is around 5 kHz for silent operation and an upper limit of 50 kHz to limit the losses in the choke and in active switching elements. The transformed wave form is rectified and filtered. A sample of the output voltage is used as the feedback signal for the drive circuit for the switching transistor to achieve regulation.



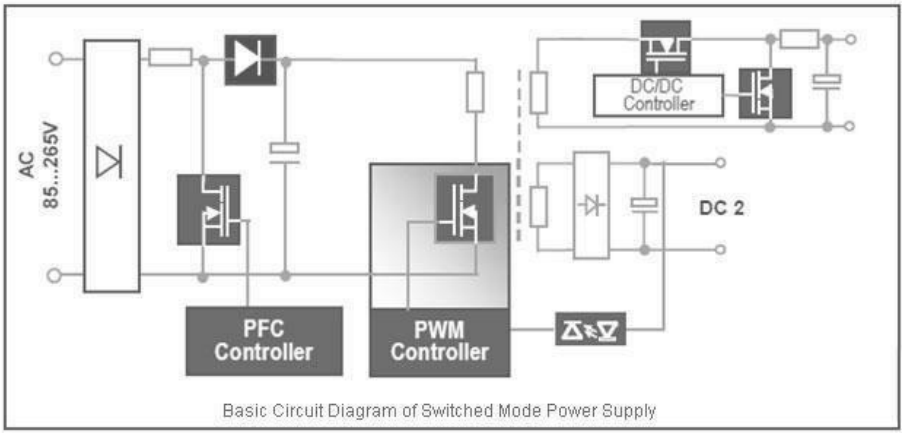
Block Diagram of Switched Mode Power Supply

The oscillator in above figure allows the control element to be switched ON and OFF. The control element usually consists of a transistor switch, an inductor, and a diode. For each switch ON, energy is pumped into the magnetic field associated with the inductor which is a transformer winding in practice. This energy is then released to the load at the desired voltage level.

By varying the duty cycle or frequency of switching, we can vary the stored energy in each cycle and thus control the output voltage. Higher efficiency is obtained since only the energy required is pumped to maintain the load current hence no power dissipation.

$$\text{Duty cycle, } \delta = \frac{T_{ON}}{T}$$

where, $T = T_{ON} + T_{OFF}$



Basic Circuit Diagram of Switched Mode Power Supply

The major feature of SMPS is the elimination of physically massive power transformers and other power line magnetic. The net result is smaller, lighter package and reduced manufacturing cost, reducing primarily from the elimination of the 50 Hz components. The basic concept of switching regulator in a simple form is shown in this figure below.

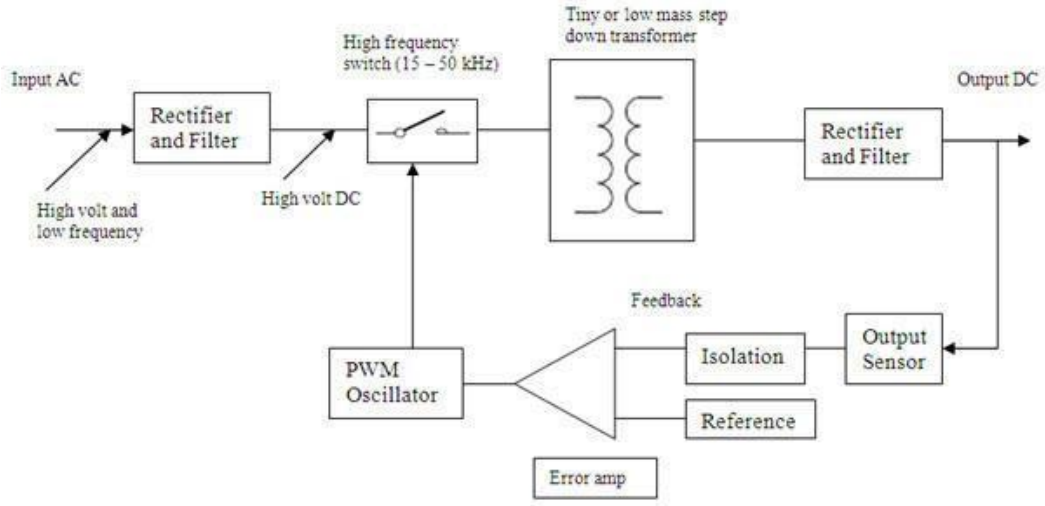
Types of SMPS:

· D.C. to D.C. Converter, Forward Converter, Flyback Converter, Self-Oscillating Flyback Converter:

D.C. to D.C. Converter

Here, the primary power received from AC main is rectified and filtered as high voltage DC. It is then switched at a huge rate of speed approximately 15 kHz to 50 kHz and fed to the primary side of the step-down transformer. The step-down transformer is only a fraction of the size of a comparable 50 Hz unit thus reliving the size and weight problems. The output at the secondary side of the transformer is rectified and filtered. Then it is sent to the output of the power supply. A sample of this output is sent back to the switch to control the output voltage.

The block diagram of D.C. to D.C. converter (**SMPS**) is shown here.



SMPS rely on PWM to control the average value of the output voltage. The average value of the repetitive pulse waveform depends on the area under the waveform. As load increases, output voltage tends to fall. Most switching power supplies regulate their output using the method called Pulse – Width Modulation (PWM). The power switch which feeds the primary of the step-down transformer is driven by the PWM oscillator. When the duty cycle is at 50%, then the maximum amount of energy will be passed through the step-down transformer. As the duty cycle decreases the power transmitted is less hence low power dissipation.

The Pulse Width signal given to the switch is inversely proportional to the output voltage. The width or the ON time of the oscillator is controlled by the voltage feedback from the secondary of the rectifier output and forms a closed loop regulator. Since switching regulator is complex, modern IC packages like Motorola MC 3420/3520 or Silicon General SG 1524 can be used instead of discrete components.

8.4 SMPS and linear power supply comparison

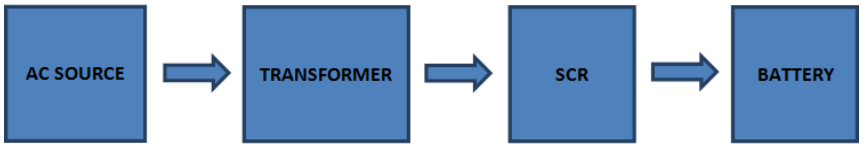
	LINEAR SUPPLY	SMPS
Size and weight	If a transformer is used, large due to low operating frequency (mains power frequency is at 50 or 60 Hz). Small if transformerless.	Smaller due to higher operating frequency (typically 50 kHz - 1 MHz)
Output voltage	With transformer used, any voltages available; if transformerless, not exceeding input. If unregulated, voltage varies significantly with load.	Any voltages available. Voltage varies little with load.
Efficiency, heat, and	If regulated, output voltage is regulated by dissipating excess power as heat resulting in	Output is regulated using duty cycle control, which draws

power dissipation	a typical efficiency of 30-40%; if unregulated, transformer iron and copper losses significant.	only the power required by the load. In all SMPS topologies, the transistors are always switched fully on or fully off.
Complexity	Unregulated may be diode and capacitor; regulated has a voltage regulating IC or discrete circuit and a noise filtering capacitor.	Consists of a controller IC, one or several power transistors and diodes as well as a power transformer, inductors, and filter capacitors.
Radio frequency interference	Mild high-frequency interference may be generated by AC rectifier diodes under heavy current loading, while most other supply types produce no high-frequency interference. Some mains hum induction into unshielded cables, problematical for low-signal audio.	EMI/RFI produced due to the current being switched on and off sharply. Therefore, EMI filters and RF shielding are needed to reduce the disruptive interference.

8.5 Schematic diagram of SCR battery charger and explain

Introduction to Battery Charger Using SCR:

The battery is charged with small amount of AC voltage or DC voltage. So if you want to charge your battery with AC source then should follow these steps, we need first limit the large AC voltage, need to filter the AC voltage to remove the noise, regulate and get the constant voltage and then give the resulting voltage to the battery for charging. Once charging is completed the circuit should automatically turned off.

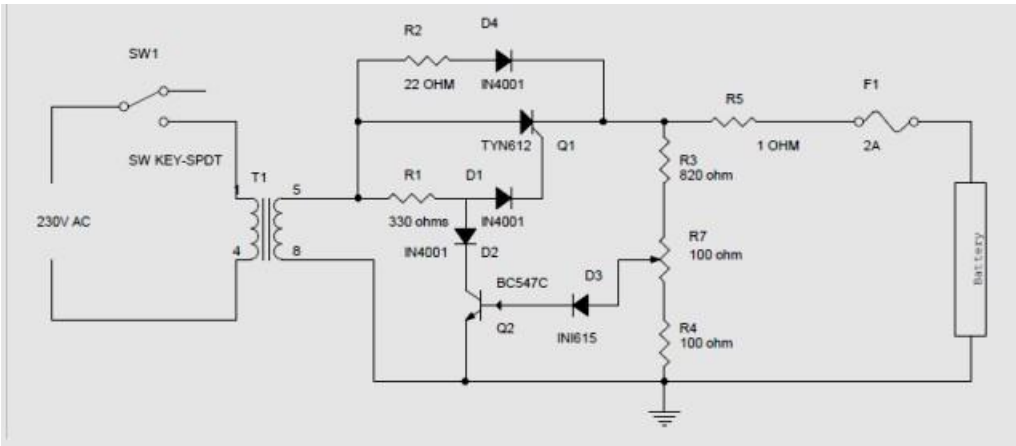


Block Diagram of Battery Charger Using SCR

The AC source is given to the step down transformer which converts the large AC source into limited AC source, filter the AC voltage and remove the noise and then give that voltage to the SCR where it will rectify the AC and give the resulting voltage to the battery for charging.

Circuit Diagram of Battery Charger Using SCR:

Circuit diagram of the Battery Charger Circuit using SCR can be seen below:



Circuit Diagram Explanation:

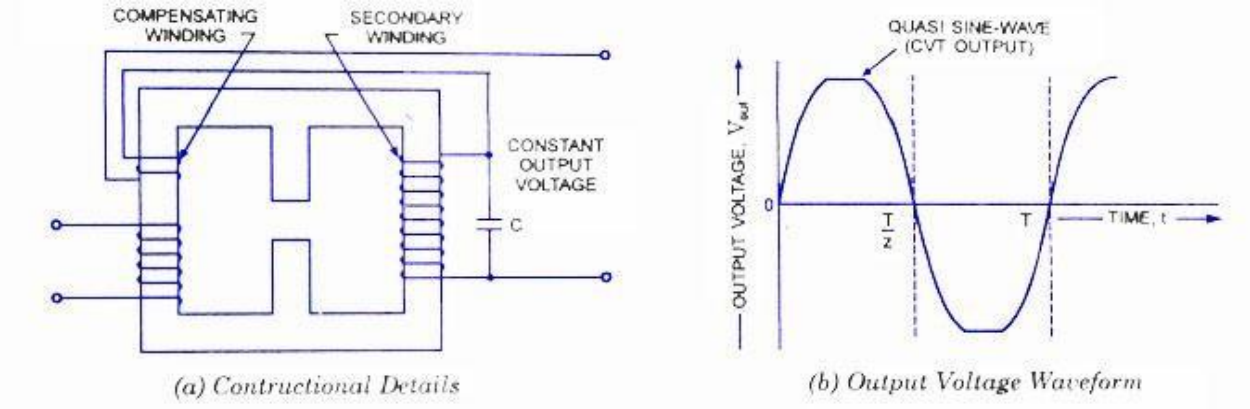
- The AC main voltage is given to the step down transformer the voltage should be down to 20V approx. the step down voltage is given to the SCR for rectification and SCR rectifies AC main voltage. This rectified voltage is used to charge battery.
- When the battery connecter to the charging circuit, the battery will not be dead completely and it will get discharged this will give the forward bias voltage to the transistor through the diode D2 and resistor R7 which will get turned on. When the transistor is turned on the SCR will get off.
- When the battery voltage is dropped the forward bias will be decreased and transistor gets turned off. When the transistor is turned off automatically the diode D1 and resistor R3 will get the current to the gate of the SCR, this will triggers the SCR and gets conduct. SCR will rectifies the AC input voltage and give to the battery through Resistor R6.
- This will charge the battery when the voltage drop in the battery decreases the forward bias current also gets increased to the transistor when the battery is completely charged the Transistor Q1 will be again turned on and turned off the SCR.

8.6 Schematic diagram of power supply using SCR for electrolytic process in industries and explain

8.7 Online UPS system and offline UPS system

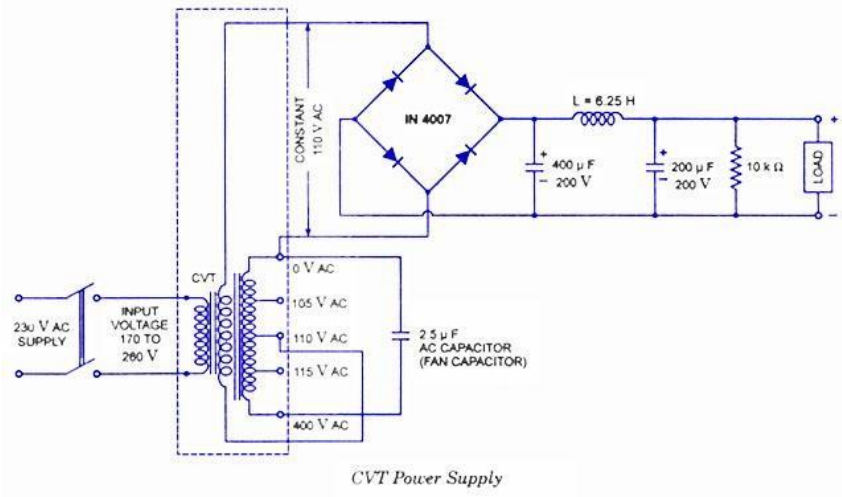
8.8 Block diagram of UPS system and its operation & application

8.9 Draw the diagram of AC servo voltage transformer (CVT) type &AC voltage stabilizer and explain its operation



(a) Contructional Details *(b) Output Voltage Waveform*

With the popularisation of PCs, the constant voltage transformers (CVTs) have also become equally popular. The CVT is simply a magnetic transformer of a special construction that has a capacitor connected across the secondary winding of the transformer. In an ordinary transformer, the primary and secondary windings are wound near each other so that whenever there is a change of voltage across the primary there is a corresponding change in the secondary voltage depending upon the ratio of the turns on the two windings. However, in a CVT the primary and secondary windings are wound separately from each other, as illustrated in figure. To set up field in between the coils, a separate shunt path is provided between the two windings but an airgap is formed in the shunt path. A capacitor is connected across suitable tappings of the secondary winding. The constructional details of a CVT are shown in the figure.



CVT Power Supply

CVT Power Supply

Operation of CVT.

The portion of the magnetic core over which the secondary winding is wound is saturated, while the portion over which the primary is wound is not saturated. A capacitor is connected across the secondary winding to tune out the output at a frequency very close to 50 Hz. This capacitor also makes the current in the secondary winding to increase which helps in the saturation of the secondary flux. Since the secondary ac flux is restricted to a saturated value for a large range of the input voltage (170-270 V), a constant voltage is available across the secondary winding. The output voltage will not be of a pure sinusoidal waveform but will be an approximate sinewave with the peaks flattened approaching a square wave. Output voltage waveform of a CVT is shown in figure. In figure, a compensating winding is shown connected in series to the secondary to improve the CVT performance.

If a CVT is placed at the output of a square wave inverter (in the UPS), care must be taken to control the frequency of the inverter, since the CVT is sensitive to the frequency of its input supply.

The reason we use a CVT and not a voltage stabilizer for computer applications is that in the voltage stabilizer relays are present and when these relays operate (switch), the output voltage may be interrupted for a short time. Such a transient may not be desirable for computers which may cause the computer to reboot. Also, the CVT provides a clean spike-free output voltage. The voltage regulation possible in a CVT also is good.

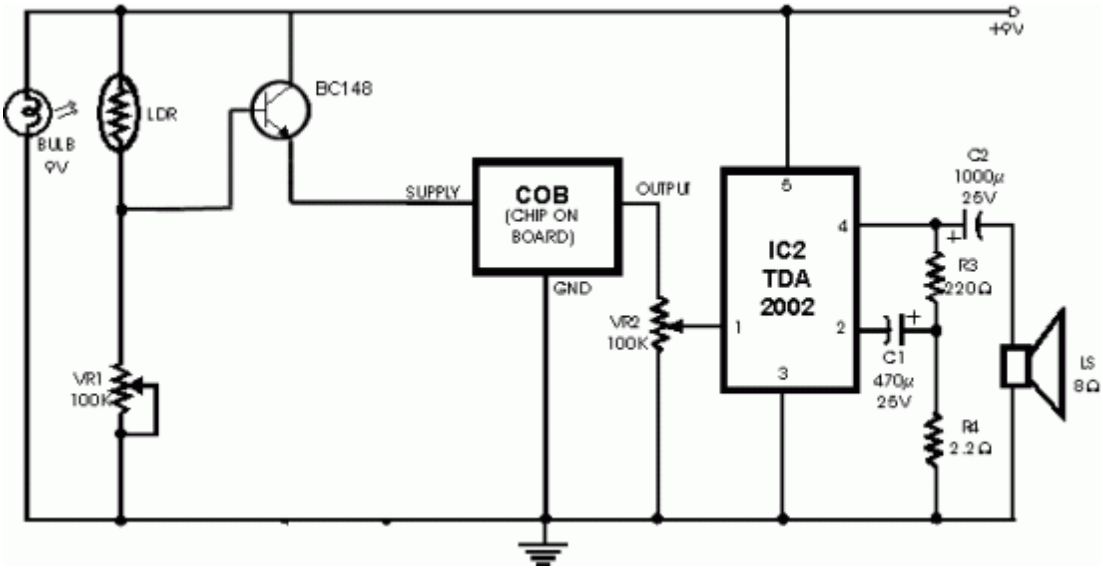
The input voltage ranges 170 to 260 V and output regulation is 230 ± 2 % at no load to full-load. Distortion-approximately 5% under full-load conditions. Rating of 50, 150, 250, 350, 500, 750, 1000, 2000 VA.

A practical circuit of a CVT power supply is given in figure.

Applications:

The CVT's are used for various applications like computers, data processing equipment, audio/video equipment, photo processing equipment, bio-medical equipment, telex, EPABX, fax, cash registers, electronic typewriters, internet application, modem & other accessories like netphone, control panels, etc.

setting of preset VR1. Thus by placing the bulb and the LDR at appropriate distances, one may vary preset VR1 to get optimum sensitivity.



(Circuit diagram of Smoke detector)

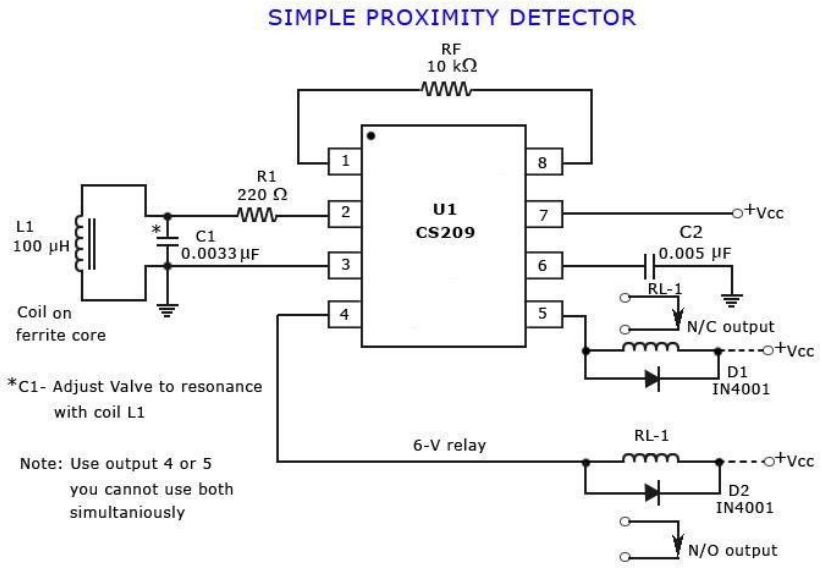
9.5 Proximity alarm circuit

This presence detector or proximity sensor circuit reacts in presence of any conductor object including humans. Sensitivity is adjustable with P1 which will be located at a great distance from the rest of the presence detector circuit. This circuit does not detect object movement but can act as an proximity sensor!

The sensitivity of the proximity sensor circuit can be adjusted with P1 for the desired ―distance‖. One of its obvious uses is to open a door automatically. For this the sensor must be placed on the front of the door.

The presence detector is made of one oscillator with T1 and a monostable. The oscillator is a Clapp one, well known for its frequency stability. The surface of the sensor acts as a capacitor for the oscillator circuit and in this configuration the frequency is around 1 MHz.

The switching time can be adjusted with P2. Do not bring metallic objects in the proximity of the circuit because if doing so the relay will stay closed! This circuit can be used as a detector of aggressive liquids, the advantage being that the surface of the sensor will not come in contact with the liquid.



(Circuit diagram of Proximity detector)

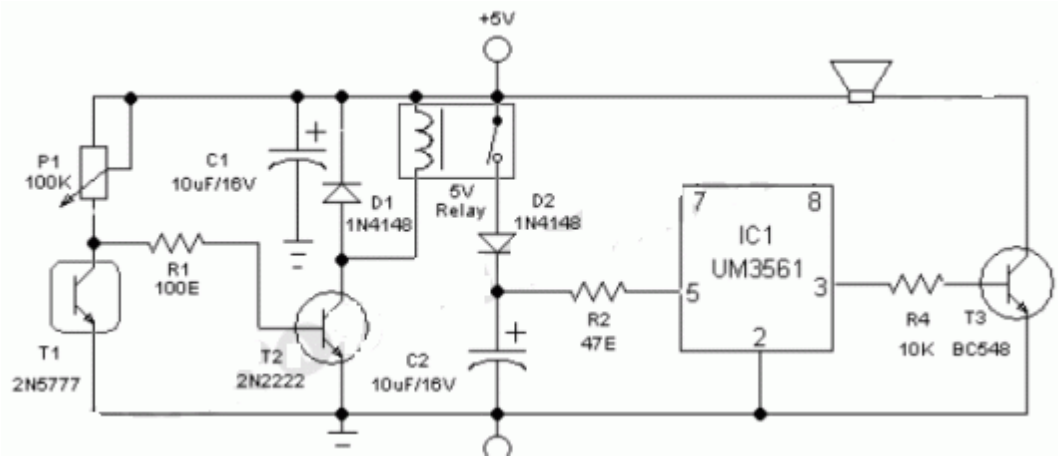
9.6 Flame failure device (flame out monitor circuit)

A minimum amount of hardware is needed to build a simple flame or fire failure monitor that enables you to monitor the status of the flame in a chamber/furnace. Owing to its integrated alarm generator, the interface can be easily adapted for use with a wide range of light/heat sensors. Here a readily available photo transistor 2N5777 (T1) works as the flame sensor. The 5V regulated dc supply for this circuit can be derived from a 12 V mains adaptor or a 9V rechargeable battery.

In the presence of the flame, T1 conducts (resistance low) and most of the base current of relay driver transistor T2 find an alternative easy path via T1. As a result T2 remains cutoff. If flame is absent, T1 behaves almost an open circuit, and the current through P1 and R1 flows into the transistor‘s (T2) base.

Next, the 5V reed relay is energised and 5V positive supply is extended to the alarm generator circuit built around the siren generator UM3561(IC1). Output signals from IC1 is amplified by transistor T2 to drive a standard 64 Ohm 1W mylar speaker.

For optimum perfomance, enclose phototransistor (T1) in a suitable long tube and add an optical assembly (see fig.2). The adjustment of sensitivity set preset pot P1 is also very critical.



(Circuit diagram of flame failure device)

9.7 Edge resister control circuit

Current measurement (i.e., monitoring current flow into and out of electronic circuits) is an essential skill for a designer and necessary in a wide range of applications. Examples of applications include overcurrent protection, 4–20mA systems, battery chargers, high-brightness LED control, GSM base station power supply, and H-bridge motor control for which you must know the ratio of current flow into and out of a rechargeable battery (that is, the gauge function).

As more applications have become portable, demand has increased for dedicated current monitors that accomplish their task in a small package and with low quiescent current. The following discussion covers low-side and high-side current monitors and includes their architectures and applications.

Most current-measurement applications employ either the low-side principle, in which the sense resistor connects in series with the ground path (Figure 1), or the high-side principle, in which it connects in series with the hot wire (Figure 2). These two approaches pose a trade-off in different areas. The low-side resistor adds undesirable extraneous resistance in the ground path. However, the circuitry associated with the high-side resistor must cope with relatively large common-mode signals. Moreover, if the op amp in Figure 1 has its GND pin referred to the positive side of RSENSE, then its common-mode input range must extend below zero, that is, to GND - (RSENSE × ILOAD).

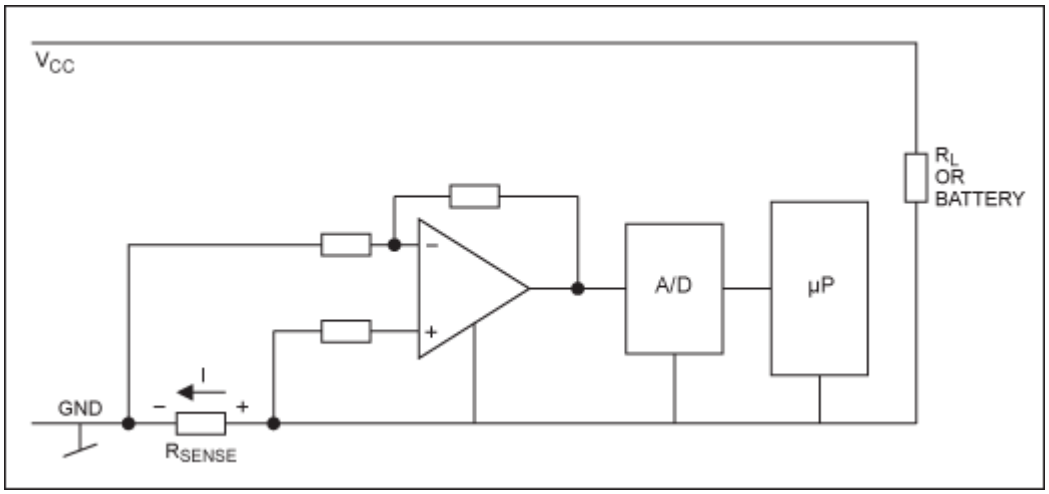


Figure 1. Principle of the low-side current monitor.

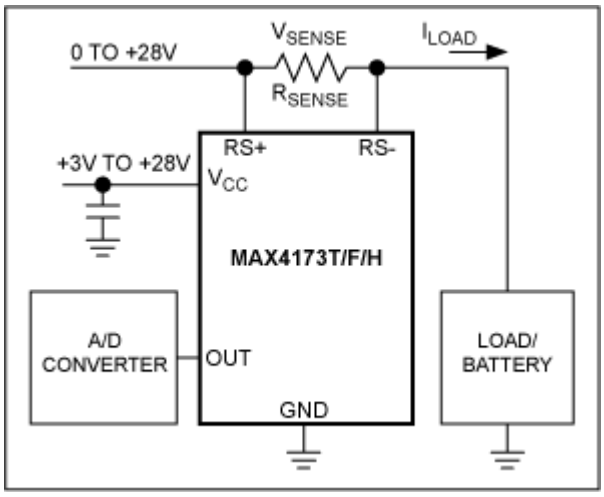


Figure 2. Example of a high-side current monitor.

9.8 Optocoupler devices and application

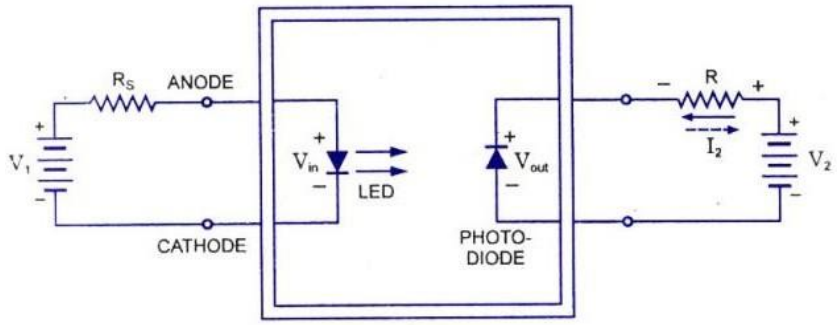
An optocoupler (or an optoelectronic coupler) is basically an interface between two circuits which operate at (usually) different voltage levels. The key advantage of an optocoupler is the electrical isolation between the input and output circuits. With an optocoupler, the only contact between the input and the output is a beam of light. Because of this it is possible to have an insulation resistance between the two circuits in the thousands of megohms. Isolation like this is useful in high voltage applications where the potentials of two circuits may differ by several thousand volts.

The most common industrial use of the optocouplers (or optically-coupled isolators) is as a signal converter between high-voltage pitot devices (limit switches etc.) and low voltage

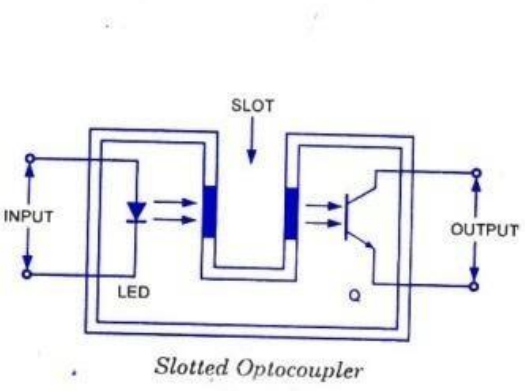
solid-state logic circuits. Optical isolators can be employed in any situation where a signal must be passed between two circuits which are isolated from each other. Complete electrical isolation between two circuits (i.e. the two circuits have no conductors in common) is often necessary to prevent noise generated in one circuit from being passed to the other circuit. This is especially necessary for the coupling between high-voltage information-gathering circuits and low-voltage digital logic circuits. The information circuits are almost badly exposed to noise sources and the logic circuits cannot tolerate noise signals.

The optocouplers works well on either ac or dc high-voltage signals. For this reason, signal converters employing optical coupling are sometimes referred to the *universal* signal converters.

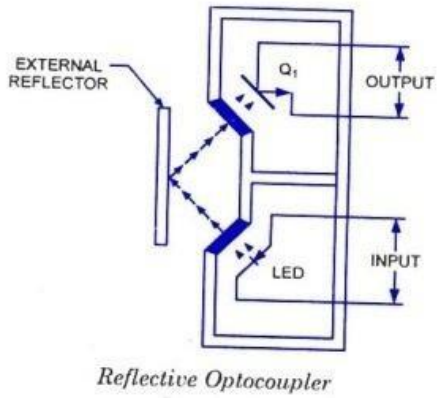
The opto-coupler is a device that contains an infra-red LED and a photodetector (such as a photodiode, phototransistor, Darlington pair, SCR or triac) combined in one package. The figure of opto- coupler is given below



Types of Optocouplers:



Slotted Optocoupler



Reflective Optocoupler

1. **Slotted Optocoupler** - A *slotted optocoupler* has a slot moulded into the package between the LED light source and the phototransistor light sensor; the slot houses transparent windows, so that the LED light can normally freely reach the face of transistor , but can be interrupted or blocked via opaque object placed within the slot. The slotted optocoupler can

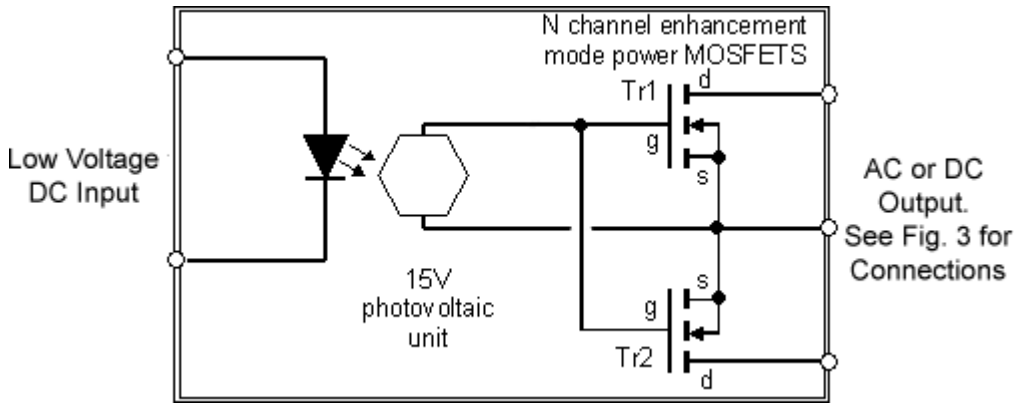
thus be employed in a variety of presence detecting applications, including end-of-tape detection, limit switching, and liquid level detection.

2. **Reflective Optocoupler** - Here the LED and phototransistor are optically screened from each other within the package, and both face outwards (in same direction) from the package. The construction is such that an optocoupled link can be set up by a reflective object (such as metallic paint or tape, or even smoke particles) placed a short distance outside the package, in line with both the LED . The reflective coupler can thus be employed in applications such as tape-position detection, engine-shaft revolution counting or speed measurement, or smoke or fog detection etc.

9.9 Solid State Relays.

Solid state relay is similar to the opto coupled devices already mentioned, but using power MOSFET transitors as the switching device. Solid State Relays (SSRs) can replace many types of low power electromechanical relays.

It uses opto−coupling to provide complete electrical isolation between its low power input circuit and its high power output circuit. When the output switch is "open" (MOSFETs off) it has a nearly infinite resistance, and a very low resistance when "closed" (MOSFETs conducting heavily). It can also be used to switch either AC or DC currents.



(A typical circuit of an SSR is shown in Figure .)

A current of about 20mA through the LED is sufficient to switch on the output MOSFETS. The (infra red) light from the LED falls on the Photovoltaic unit) which comprises 25 silicon diodes. Each diode produces 0.6V to give the 15V gate potential needed to turn on the MOSFETS. Figure 2 represents a basic example of a SSR, in this case the Siemens LH1540T

Advantages

- Slimmer profile, allowing tighter packing.
- Totally silent operation
- SSRs are faster than electromechanical relays; their switching time is dependent on the time needed to power the LED on and off, of the order of microseconds to milliseconds
- Increased lifetime, even it is activated many times, as there are no moving parts to wear and no contacts to pit or build up carbon
- Output resistance remains constant regardless of amount of use

PROGRAMMABLE LOGIC CONTROLLERS

INTRODUCTION:-

A programmable logic controller (PLC) is a specialized computer used to control machines and processes. It uses a programmable memory to store instructions and execute specific functions that include on/off control, Timing, Counting, Sequencing, arithmetic and data handling. Programmable logic controllers are used for the control and operation of manufacturing process equipment and machinery.

PARTS OF A PLC:-

- A typical PLC can be divided into parts as illustrated in the Figure below. These components are the central processing unit (CPU), the input /output (I/O) section, the power supply and the programming device.
- The term architecture can refer to PLC hardware to PLC software, or to a combination of both.

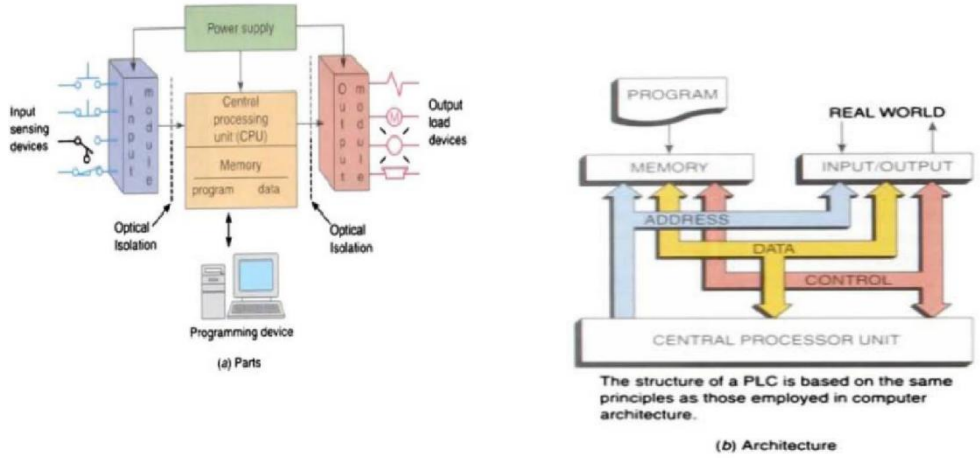
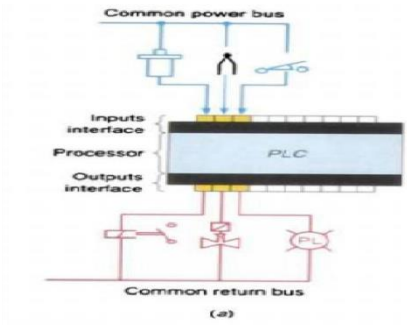
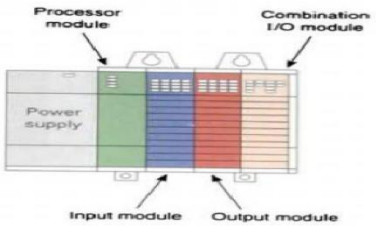


FIGURE: - PLC parts and architecture

- There are two ways in which I/O is incorporated into the PLC: fixed and modular.
- Fixed I/ O is typical of small PLCs that come in one package with no separate, removable units. The processor and I/O are packaged together, and the I/O terminals are available but cannot be changed.
- The main advantage of this type of packaging is lower cost.
- One disadvantage of fixed I/O is its lack of flexibility.





(b)

FIGURE: I/O configurations: (a) fixed I/O (b) modular I/O

- Modular I/O in figure shown above is divided by compartments into which separate modules can be plugged. This feature greatly increases your options and the unit's flexibility. The basic modular controller consists of a rack, power supply, processor module (CPU), input/output (l /O modules), and an operator interface for programming and monitoring. The modules plug into a rack. When a module is slid into the rack, it makes an electrical connection with a series of contacts called the backplane, located at the rear of the rack.
- The power supply supplies dc power to other modules that plug into the rack. For large PLC systems, this power supply does not normally supply power to the field devices. With larger systems, power to field devices is provided by external alternating current (ac) or direct current (dc) supplies.
- The processor (CPU) is the "brain" of the PLC. A processor usually consists of a microprocessor for implementing the logic and controlling the communications among the modules. The processor requires memory for storing the results of the logical operations performed by the microprocessor. Memory is also required for the program EPROM or EEPROM plus RAM.
- The I/O section consists of input modules and output modules (Fig. shown below). The I/O system forms the interface by which field devices are connected to the controller. The purpose of this interface is to condition the various signals received from or sent to external field devices. Input devices such as pushbuttons, limit switches, sensors, selector switches, and thumbwheel switches are hardwired to terminals on the input modules. Output devices such as small motors, motor starters, solenoid valves, and indicator lights are hardwired to the terminals on the output modules.

FIGURE: (a) Typical input module (b) typical output module

- The programming device, or terminal, is used to enter the desired program into the memory of the processor. This program is entered using relay ladder logic, which is the most popular programming language used by all major manufacturers of PLCs. Ladder logic programming language uses instead of words, graphic symbols that show their intended outcome. It is a special language written to make it easy for people familiar with relay logic control to program the PLC.

THE I/O SECTION:-

- The I/O section consists of an I/O rack and individual I/O modules similar to that shown in Figure shown below. Input interface modules accept signals from the machine or process devices and convert them into signals that can be used by the controller. Output interface modules convert controller signals into external signals used to control the machine or process.

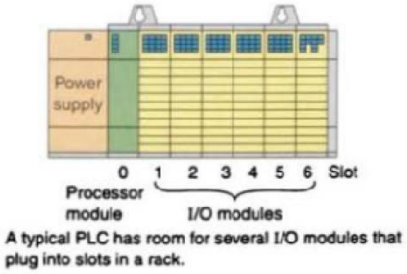
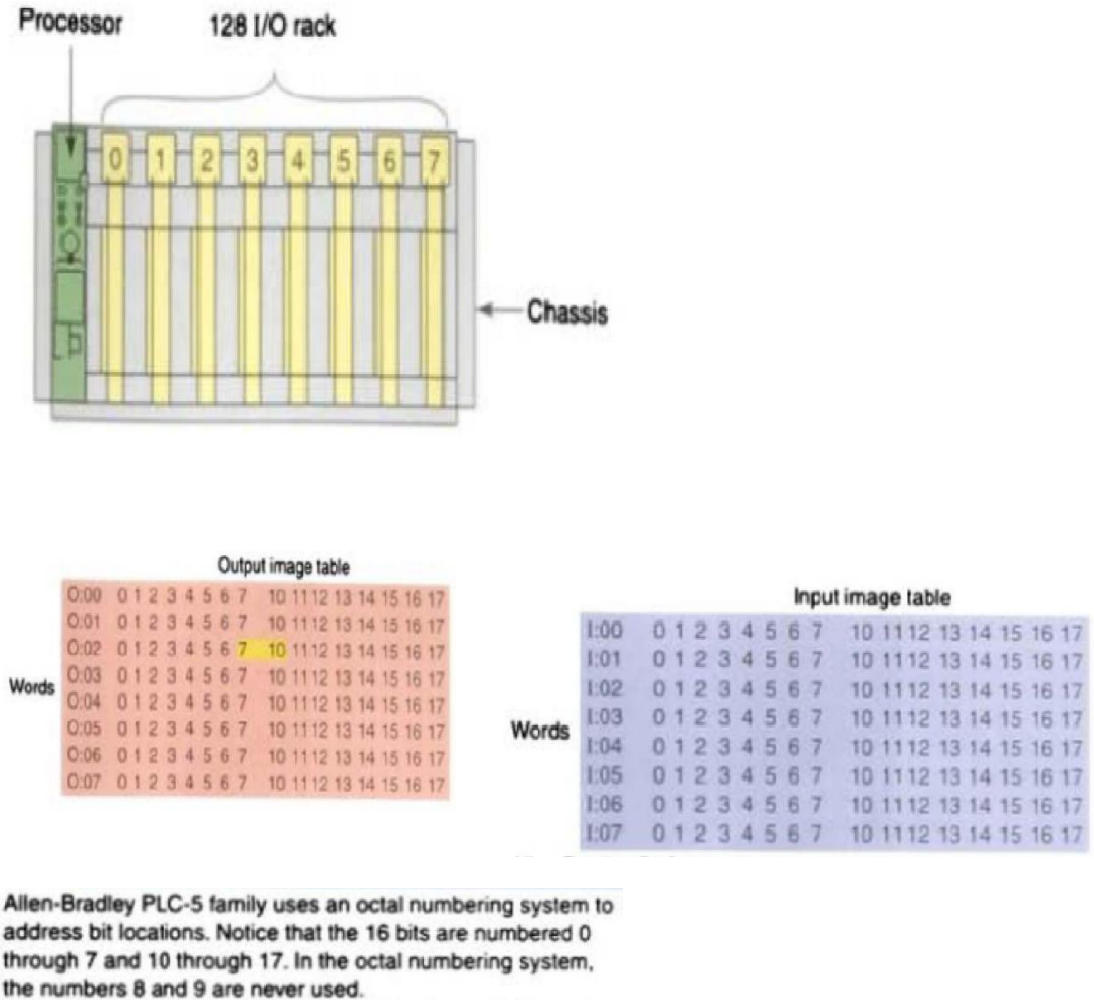


Figure: I/O section

- The I/O system provides an interface between the hardwired components in the field and the CPU. The input interface allows status information regarding processes to be communicated to the CPU, and thus allows the CPU to communicate operating signals through the output interface to the process devices under its control.

- A chassis is a physical hardware assembly that houses devices such as I/O modules, processor modules, and power supplies. Chassis come in different sizes according to the number of slots they contain. In general, they can have 4, 8, 12, or 16 slots.
- A logical rack is an addressable unit consisting of 128 input points and 128 output points. A rack uses 8 words in the input image table file and 8 words in the output image table file. A word in the output image table file and its corresponding word in the input image table file are called an I/O group. A rack can contain a maximum of 8 I/O groups (numbered from 0 through 7) for up to 128 discrete I/O (Fig. shown below). There can be more than one rack in a chassis and more than one chassis in a rack.

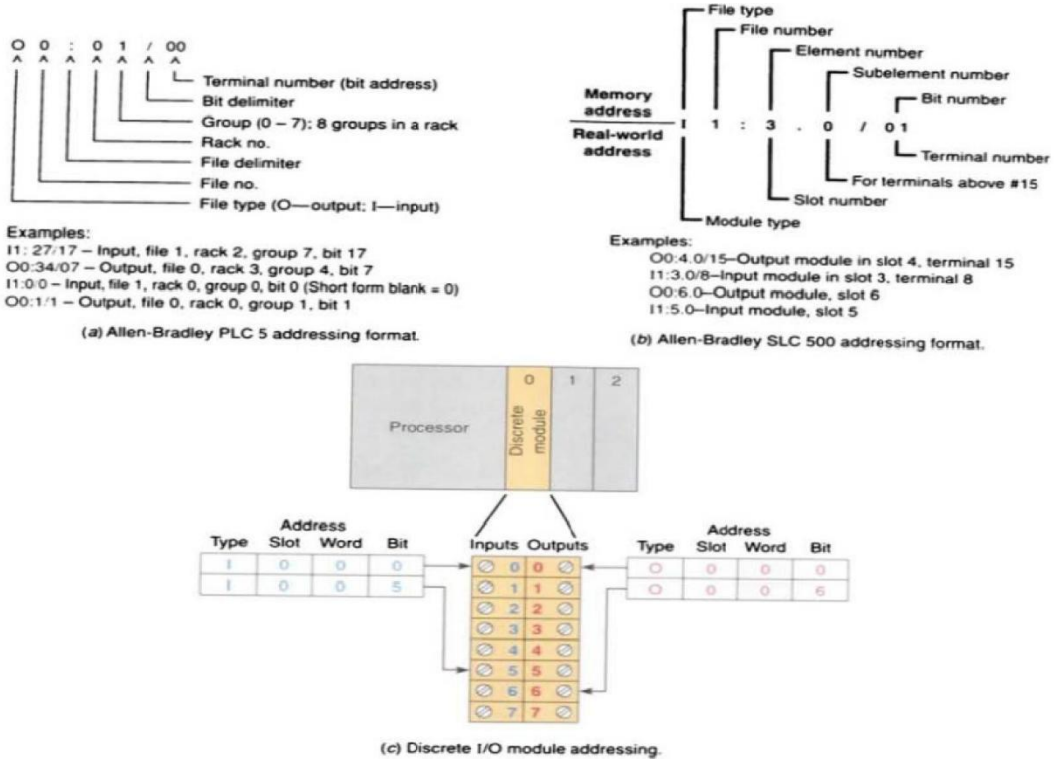


Allen-Bradley PLC-5 family uses an octal numbering system to address bit locations. Notice that the 16 bits are numbered 0 through 7 and 10 through 17. In the octal numbering system, the numbers 8 and 9 are never used.

Figure: Logical rack

- One benefit of a PLC system is the ability to locate the I/O modules near the field devices to minimize the amount of wiring required. This rack is referred to as a remote rack when it is located away from the processor module.
- The location of a module within a rack and the terminal number of a module to which an

input or output device is connected will determine the device's address (Fig. shown below). Each input and output device must have a specific address. This address is used by the processor to identify where the device is located to monitor or control it. In addition there is some means of connecting field wiring on the I/O module housing. Connecting the field wiring to the I/O housing allows easier disconnection and reconnection of the wiring to change modules. Lights are also added to each module to indicate the ON or OFF status of each I/O circuit. Most output modules also have blown fuse indicators.



In general, basic addressing elements include:

- **TYPE**

  The type determines if an input or output is being addressed.

- **SLOT**

  The slot number is the physical location of the I/O module. This may be a combination of the rack number and the slot number when using expansion racks.

- **WORD AND BIT**

  The word and bit are used to identify the actual terminal connection in a particular I/O module. A discrete module usually uses only one word, and each connection corresponds to a different bit that makes up the word.

PLC MEMORY ORGANIZATION:-

- The term processor memory organization refers to how certain areas of memory in a given PLC are used.

Figure given below shows an illustration of the Allen-Bradley PLC-2 memory organization, known as a memory map. Every PLC has a memory map, but it may not be like the one illustrated. The memory space can be divided into two broad categories: the user program and the data table. The individual sections, their order, and the sections' length will vary and may be fixed or variable, depending on the manufacturer and model.

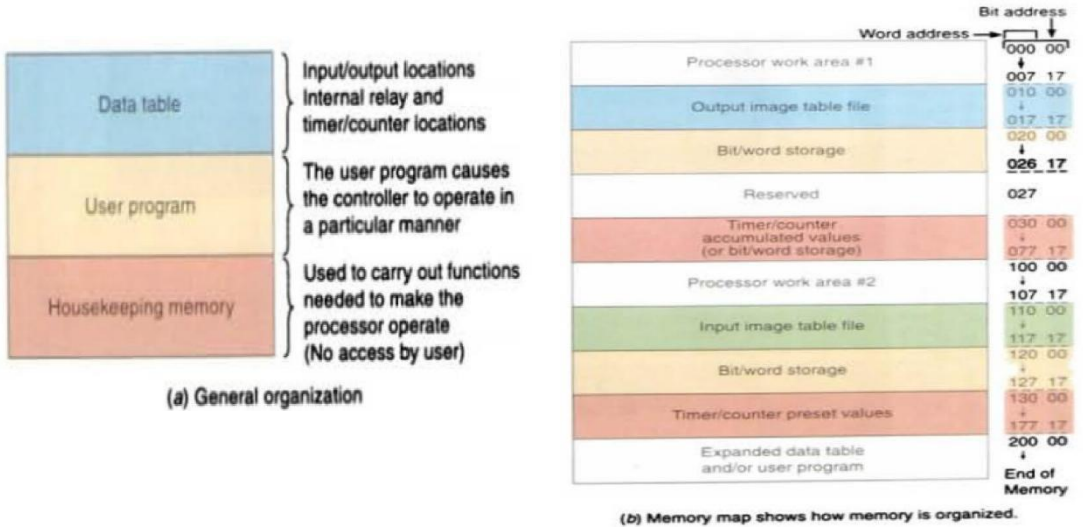


Figure: Memory map for an Allen-Bradley PLC-2

- The user program is where the logic ladder program is entered and stored. The user program will account for most of the total memory of a given PLC system. It contains the logic that controls the machine operation. This logic consists of instructions that are programmed in a ladder logic format. Most instructions require one word of memory.
- The data table stores the information needed to carry out the user program. This includes information such as the status of input and output devices, timer and counter values, data storage, and so on. Contents of the data table can be divided into two categories: status data and numbers or codes. Status is ON/OFF type of information represented by 1s and 0s, stored in unique bit locations. Number or code information is represented by groups of bits that are stored in unique byte or word locations.
- A processor file is the collection of program files and data files created under a particular processor file name. It contains all the instructions, data, and configuration information pertaining to a user program.

Figure shown below shows typical program and data file memory organization for an Allen-Bradley SLC-500 controller. The contents of each file are outlined in the sections that follow.

Program files:-

Program files are the areas of processor memory where ladder logic programming is stored. They may include:

- **System functions (file 0) -** This file is always included and contains various system-related information and user programmed information such as processor type. I/O configuration processor files name, and password.
- **Reserved (file 1)-**This file is reserved by the processor and is not accessible to the user.
- **Main ladder program (file 2) -** This file is always included and contains user programmed instructions that define how the controller is to operate.
- **Subroutine ladder program (files3- 255)-**These files are user-created and are activated according to subroutine instructions residing in the main ladder program file.

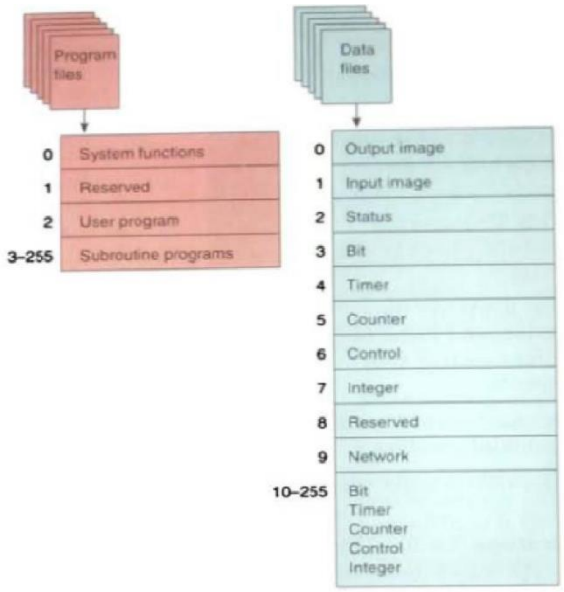


Figure: Program and data file memory organization for an Allen-Bradley SLC-500 controller

Data Files:-

The data file portion of the processor's memory stores input and output status, processor status, the status of various bits, and numerical data. All this information is accessed via the ladder logic program. These files are organized by the type of data they contain and may include:

- **Output (file 0) -** This file stores the state of the output terminals for the controller.
- **Input (file 1)**-This file stores the status of the input terminals for the controller.
- **Status (file 2) -** This file stores controller operation information. This file is useful for troubleshooting controller and program operation.
- **Bit (file 3)**-This file is used for internal relay logic storage.

- **Timer (file 4)**-This file stores the timer accumulated and preset values and status bits.
- **Counter (file 5)**-This file stores the counter accumulated and preset values and status bits.
- **Control (file 6)**-This file stores the length, pointer position, and status bit for specific instructions such as shift registers and sequencers.
- **Integer (file 7)-**This file is used to store numerical values or bit information.
- **Reserved (file 8)** - This file is not accessible to the user.
- **Network communications (file 9) -** This file is used for network communications if installed or used like files 10-255.
- **User-defined (files 10-255)**-These files are user-defined as bit, timer, counter, control, and/or integer data storage.

PROGRAM SCAN OF A PLC:-

- During each operating cycle, the processor reads all the inputs, takes these values, and energizes or de-energizes the outputs according to the user program. This process is known as a scan. Figure shown below shows a single PLC scan, which consists of the I/O scan and the program scan. Because the inputs can change at any time, the PLC must carry on this process continuously.

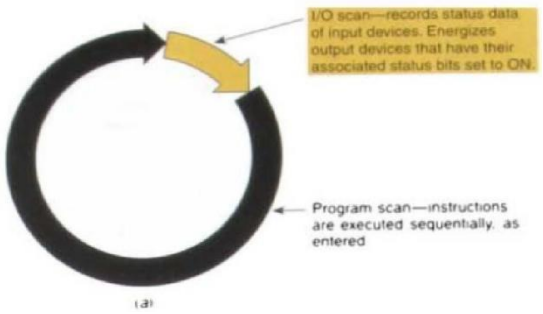


Figure: Single PLC scan

- The PLC scan time specification indicates how fast the controller can react to changes in inputs. Scan time varies with program content and length. The time required to make a single scan can vary from about 1 ms to 20 ms. If a controller has to react to an input signal that changes states twice during the scan time, it is possible that the PLC will never be able to detect this change.
- For example, if it takes 8 ms for the CPU to scan a program, and an input contact is opening and closing every 4 ms, the program may not respond to the contact changing state. The CPU will detect a change if it occurs during the update of the input image table file, but the CPU will not respond to every change. The scan is normally a continuous and sequential process of reading the status of inputs, evaluating the control logic, and updating the outputs.

Figure shown below illustrates this process.

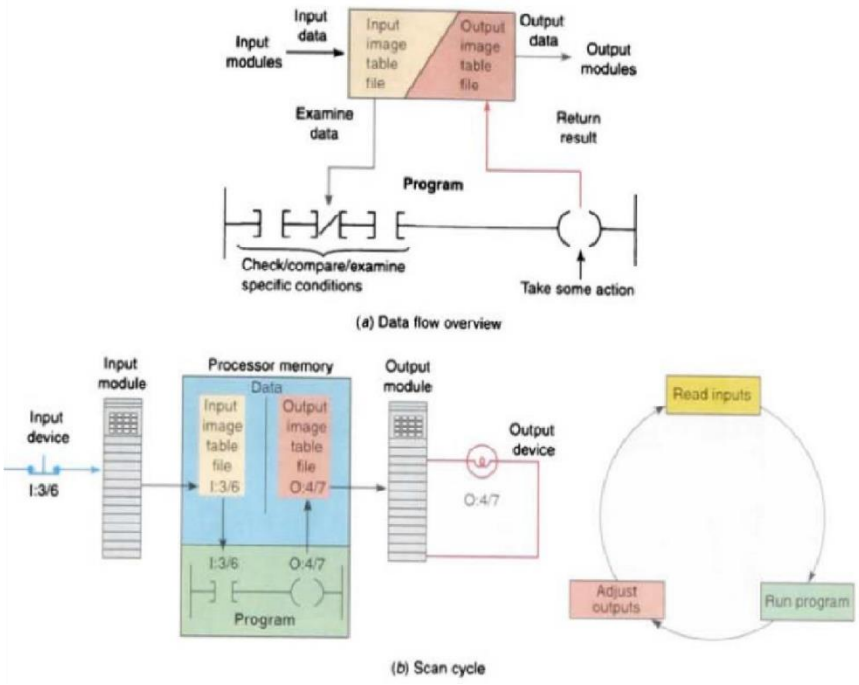
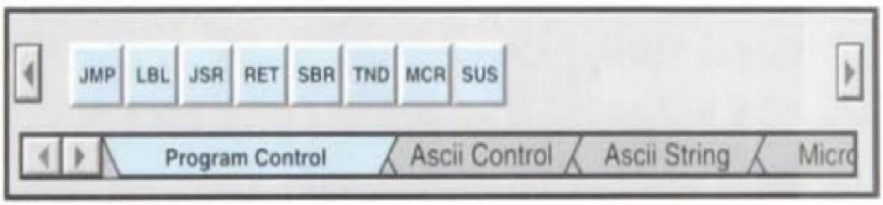


Figure: Scan Process

- When the input device connected to address I:3/6 is closed, the input module circuitry module circuitry senses a voltage and a 1 (ON) condition is entered into the input image table bit I:3/6. During the program scan, the processor examines bit I: 3/6 for a 1 (ON) condition.
- In this case, because input I: 3/6 is 1, the rung is said to be TRUE. The processor then sets the output image table bit O: 4/7 to 1. The processor turns on output O: 4/7 during the next I/O scan, and the output device (light) wired to this terminal becomes energized. This process is repeated as long as the processor is in the RUN mode. If the input device were to open, a 0 would be placed in the input image table. As a result, the rung would be called FALSE. The processor would then set the output image table bit O: 4/7 to 0, causing the output device to turn off.

CONTROL INSTRUCTIONS OF PLC:-

- Figure given below shows typical program control instructions.
- Instructions comprising the override instruction group include the master control reset (MCR) and jump (JMP) instructions.
- These operations are accomplished by using a series of conditional and unconditional branches and return instructions.



Command	Name	Description
JMP	Jump to Label	Jump forward/backward to a corresponding label instruction
LBL	Label	Specifies label location
JSR	Jump to Subroutine	Jump to a designated subroutine instruction
RET	Return from Subroutine	Exits current subroutine and returns to previous condition
SBR	Subroutine	Identifies the subroutine program
TND	Temporary End	Makes a temporary end that halts program execution
MCR	Master Control Reset	Clears all set outputs between the paried MCR instructions
SUS	Suspend	Identifies specific conditions for program debugging and system troubleshooting

- Hardwired master control relays are used in relay circuitry to provide input/output power shutdown of an entire circuit. Figure shown below is a typical hardwired master control relay circuit. In this circuit, unless the master control relay coil is energized, there is no power flow to the load side of the MCR contacts. The master control relay circuit shown in Figure below could not be programmed into the PLC as it appears because it contains two vertical contacts. For this reason, most PLC manufacturers include some form of master control relay as part of their instruction set. These instructions function in a similar manner to the hardwired master control relay; that is, when the instruction is true, the circuit functions normally, and when the instruction is false, outputs are switched off. Because these instructions are not hardwired but programmed, for safety reasons they should not be used as a substitute for a hard· wired master control relay, which provides emergency I/O power shutdown

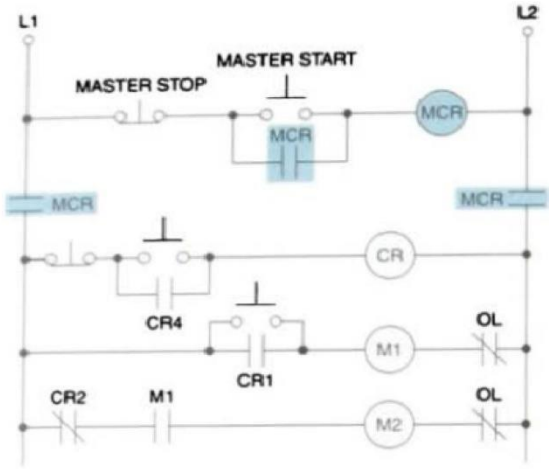


Figure: Hardwired master control relay circuit

- The master control reset instruction can be programmed to control an entire circuit or to control only selected rungs of a circuit. In the program of figure shown below, the MCR is programmed to control an entire circuit. When the MCR instruction is false, or de-energized, all non retentive (nonlatched) rungs below the MCR will be de-energized even if the programmed logic for each rung is true. All retentive rungs will remain in their last state. The MCR instruction establishes a zone in the user program in which all nonretentive outputs can be turned off simultaneously. Therefore, retentive instructions should not normally be placed within an MCR zone because the MCR zone maintains retentive instructions in the last active state when the instruction goes false.

DIFFERENCE BETWEEN PLC AND PC:-

PLC:-

- The input- output capabilities are large and can be used in various industrial processes.
- The input-output cards are mounted on racks and are visible.
- The noise is more.
- The possibility of mishap exists as input-output cards are on the rack.
- The connections are rugged, accessible and organized.
- The processor architecture is simple.
- It is used for controlling industrial processes and control logic programming.
- The interface is by using simple devices such as indicators push buttons etc.
- It uses ladder programming.
- It has limited expandability.

PC:-

- Limited input-output capabilities interms of analog and digital cards which are suited for laboratory purposes.

- The input-output cards are mounted on board and are not visible.
- Noise is less
- No possibility of mishap
- There exists a bunch of cables and very small room available for cable connections.
- The processor architecture is complicated.
- It is used for many advanced computation and high level programming language is used.
- The easy and good interface is not possible.
- It uses microprocessor programming
- It has great flexibility and high reliability.

LADDER RUNG DIAGRAM:-

- The main function of the ladder logic diagram program is to control outputs based on input conditions. This control is accomplished through the use of what is referred to as a ladder rung. In general, a rung consists of a set of input conditions, represented by contact instructions, and an output instruction at the end of the rung, represented by the coil symbol (Fig. given below).

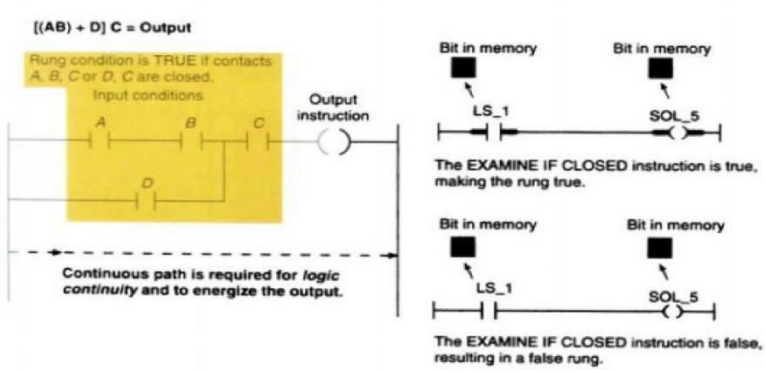


Figure: Ladder rung

- Each contact or coil symbol is referenced with an address number that identifies what is being evaluated and what is being controlled. The same contact instruction can be used throughout the program whenever that condition needs to be evaluated.
- For an output to be activated or energized, at least one left-to-right path of contacts must be closed. A complete closed path is referred to as having logic continuity.
- When logic continuity exists in at least one path, the rung condition is said to be TRUE. The rung condition is FALSE if no path has continuity.
- During controller operation, the processor determines the ON/OFF state of the bits in the data files, evaluates the rung logic, and changes the state of the outputs according to the logical continuity of rungs. More specifically, input instructions set up the conditions under which the processor will make an output instruction true or false.
- These conditions are as follows:
    1. When the processor finds a continuous path of true input instructions in a rung, the

OUTPUT ENERGIZE [OTE] output instruction will become (or remain) true. We then say that rung conditions are TRUE.

2. When the processor does not find a continuous path of true input instructions in a rung, the OTE input instruction will become (or remain) false. We then say that rung conditions are FALSE.

TIMER:-

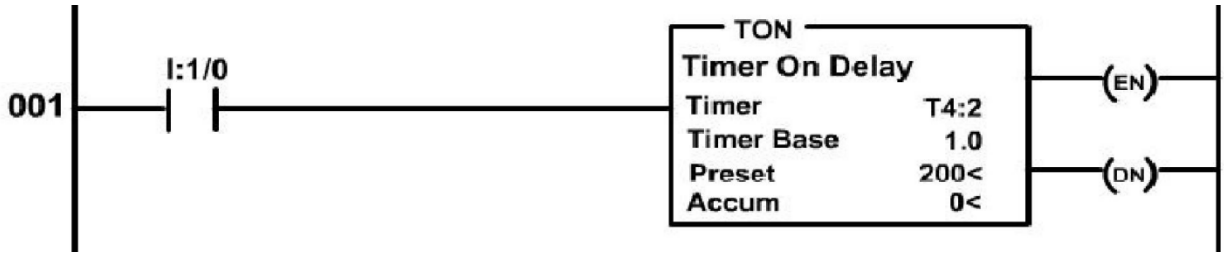
All PLC's have timer instructions. Timers are output instructions that are internal to the programmable logic controller. Timers provide timed control of the devices that they activate or de-activate.

Basic functions of timer

- Timers are used to delay an action.
- Timers are used to run an operation for a predetermined period of time.
- Timers are also used to record the total accumulated time of continuous or intermediate events.

Timer's Instructions:-

Timers consists of following parts: timer address, preset value, timer base, and accumulated value, as shown in figure below.



In the above figure, term instruction name is timer on delay (TON), timer base is 1.0 seconds, timer address is T4:0, accumulated value of zero (0) and a preset value of 200. Each timer instruction has three very useful status bits. These bits are timer enable (E N), timer timing (TT), and timer done (DN). There are 3 types of timers: On- delay timer, Off-delay timer, and retentive timer.

On delay timer:-

- Use this instruction to program a time delay after instructions become true.
- On – delay timers are used when an action is to begin a specified time after the input becomes true. For example, a certain step in the manufacturing is to begin 45 seconds after a signal is received from a limit switch. The 45- seconds delay is the on-delay timers preset value.

Off- delay timer:-

- Off- delay timer instructions is used to program a time delay to begin after rung input goes false.
- As an example, when an external cooling fan on a motor is provided, the fan has to run all the time the motor is running and also for certain time (say 10min) after the motor is turned off. This is a ten minute off- delay timer. The ten-minute timing period begins as soon as the motor is turned off.

Retentive timer:-

- Retentive timer is a timer which retains the accumulated value in case of power loss, change of processor mode or rung state going from true to false (rung state transition).
- Retentive timer can be used to track the running time of a motor for its maintenance purpose. Each time the motor is turned off, the timer will remember the motor's elapsed running time. The next time the motor is turned on, the time will increase from there. This timer can be reset by using a reset instruction.

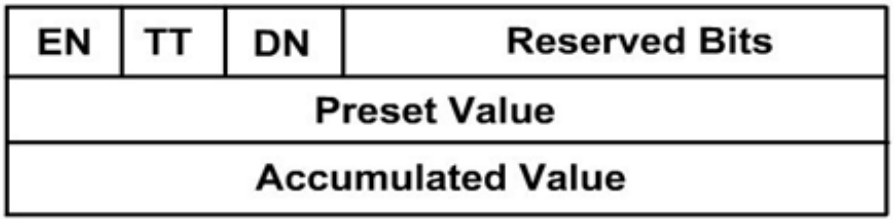
Reset:-

- This instruction is used to reset the accumulated value of counter or timer.
- It is used to reset a retentive timer's accumulated value to zero.

A typical timer element:-

A timer element is made up of three 16 bit words:

- Word 0: 3 status bits (EN, TT, DN).
- Word 1: Preset values.
- Word 2: Accumulated value.



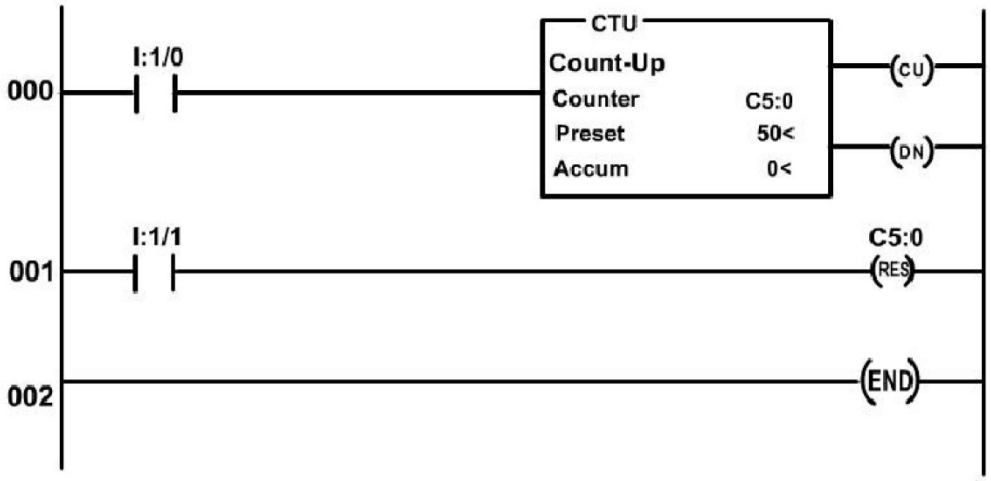
COUNTER:-

A counter is a simple device intended to do one simple thing-count. Every PLC has counter instructions. Using counters sometimes be little challenging because many manufacturers seem to use them different way. In other words, the instruction symbol used and method of programming will change for different manufacturers.

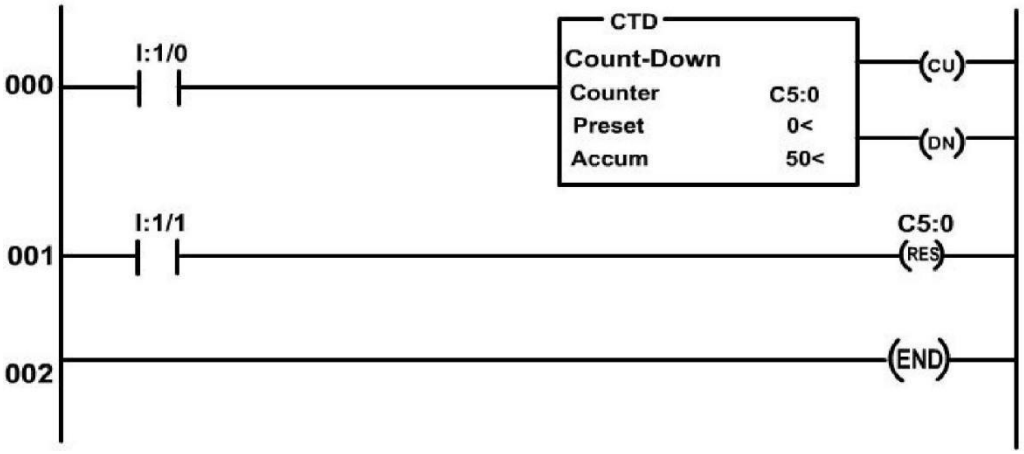
A typical counter counts from 0 up to a predetermined value, called the "preset" value. For example, if you wanted to count from certain value, say from 0 to 50, you would be counting

up using a count-up or up-counter. Here, the number "50" is the predetermined value, which is nothing but preset value. The current count or accumulated count is called as the "accumulated value". If our counter had counted 25 pieces that had passed on the conveyor, the accumulated count would be 25. When all 50 pieces had passed on the conveyor, the preset value and counter accumulated value would be equal. At this point the counter would signal other logic within the PLC program that the batch of 50 was completed and it should now take some action. The next action the PLC has to take is to move the box containing 50 parts on to the next station for carton sealing. To start counting the next batch, a reset instruction would be used to reset the counter's accumulated value back to zero.

The fig below shows an up-counter, counting from 0 to 50.



The fig below shows a down-counter, counting from 50 to 0.



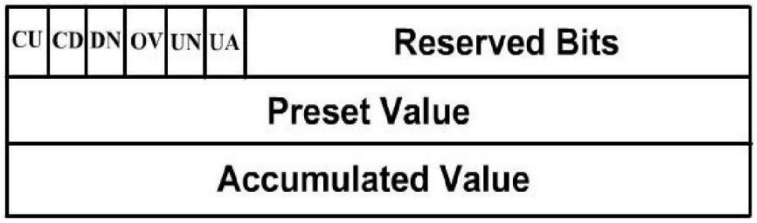
PLC Counter Instructions

Instruction	This instruction is used to	Functional description
Count Down	Count down from a desired value to zero	An operator interface display shows the operator the number of parts remaining to be made for a lot of,say 50 parts ordered.
Count Up	Count from zero up to a desired value	Counting the number of parts produced during a specific work shift or batch.Also counting the number of rejects from a batch.
High-speed Counter	Count input pulses that are too fast,from normal input points and modules	Most fixed programmable logic controllers have a high-speed set of input points that allow interface to high-speed inputs. Signals from an incremental encoder would be a typical high-speed input.
Counter Reset	To reset a counter or timer	Used to reset a counter to zero so that another counting sequence can begin.

As for explanation, let us take ALLEN-BRADELY counters:

In Allen-bradely counter, the default counter file is file 5. The counter data is stored in counter file. Each counter consists of three 16-bit words and is known as "counter element". In a single processor file, there can be many counter files. Any data file, which is greater than file 8 can be assigned as an additional counter file. Each counter file can have up to 256 counter elements. A counter instruction is one element. A counter element is made up of three 16-bit words. Thus, the counter instruction contains the three parts i.e. word0, word1 and word2.

- Word zero is for status bits. Status bits include CU, CD, DN, OV, UN, and UA. Along with their associated instructions.
- Word one is for the preset value.
- Word two is for accumulated value.



Addressing a counter

1) To address the counter as a unit the addressing format used is C5:4.
Where, C= C identifies this as a counter file.
5= This is counter file 4 which is default. Any unused file from 10 to 255 can be assigned to counters.
:4= The colon used here is called the file separator. It separates the file, file 5, from the specific counter, in this case, counter 4 in counter file 5.
2) To address the counter 14's accumulated value, the address used is C5:14.ACC.
Where, C= C identifies this as a counter file.
5= This represents the counter file 5.
:14= The colon is called the file separator. The colon separates the file, file 5, from the specific counter; in this case, counter 14 in counter file 5.
. = The point is called the word delimiter. The word delimiter is used to separate the counter number, called the structure, from the sub element. The sub element is ACC for the accumulated value. Similarly, preset value can be accessed as C5:14.PRE.

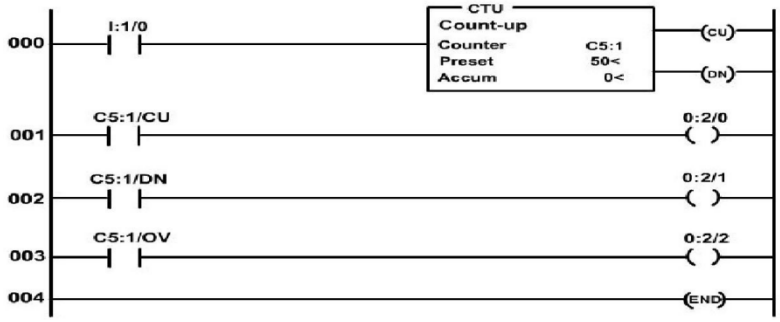
The addressing format of counter status bits is as follows:

- C5:14/DN is the address for counter file 5, counter 14's done bit.
- C5:14/CU is the address for counter file 5, counter 14's count-up-enable bit.
- C5:14/EN is the address for counter file 5, counter 14's enable bit.

Working of a counter:-

- A counter instruction is always an output instruction. The counter instruction counts each time the input logic changes the rung state from false to true. This input logic can be signal from an external device, for e.g. limit switch or sensor, or a signal from internal logic. Every time the counter instruction sees a false-to-true rung transition, a count-up counters accumulated value is incremented by one.
- The working of down-counter is little different. Each time when count-down counter sees a false-to-true rung transition, its accumulated value is decremented by one. Since the accumulated value gets decremented by 1 when each time the input logic changes the rung state from false to true, the accumulated value must be chosen as the starting point of the count.
- Counters are retentive in nature. The counter will retain its accumulated value or the on or off status of the done, overflow and underflow bits through a power loss.

The count-up instruction



The count-up instruction is used if we want a counter to increment one decimal value each time it register a rung transition from false to true. Each time input I:1/0 has a transition from off to on, counter C5:1 will increment its accumulated value by one decimal value. The count-up-enabled bit, on rung 001 is set when the rung conditions are true, or enabled. In rung 002, the done bit, DN, is set when the accumulated value is equal to or greater than the preset value. In the event of wrap from +32,767 to -32,768, the accumulated value becomes less than the preset value and the done bit will not be reset. In rung 003, the count-up overflow bit, OV, is set whenever the count-up counters accumulated value wraps from +32,767 to -32,768.

The count-down instruction

This instruction is used when we want to count down over the range of +32,767 to -32,768. Accumulated value will be decremented by one count, each time the instruction sees a false-to-true transition. Count-down instruction has many applications, for example: if we want to display the remaining number of parts to be filled for a specific order say 50 parts, then, a count-down instruction can be used. In this example, the accumulated value will be set as 50 and the preset value will be 0. Each time a part is completed and passes the sensor, the accumulated value will be decremented by one decimal value, as shown in the figure below.